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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ohad Falik, et al.
Serial No.:	09/810,746
Filed:	March 16, 2001
For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicants herewith respectfully submit that the Examiner's decision of July 26, 2005, finally rejecting Claims 2, 4-6, 50-60, 70, 71, and 74 in the present application, should be reversed, in view of the following arguments and authorities. This Brief is submitted on behalf of Appellant for the application identified above. A check is enclosed for the fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

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TABLE OF AUTHORITIES

ACS Hospital Systems v. Montefiore Hospital, 220 USPQ 929 (Fed.Cir. 1984). 33

Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966). 7

In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed.Cir. 1990). 33

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SRI Int'l v. Matsushita Elec. Corp. of America, 775 F.2d 1107, 227 U.S.P.Q. 577 (Fed. Cir. 1985). 7

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Real Party in Interest

The real party in interest, and assignee of this case, is National Semiconductor Corporation.

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

Status of Claims

Claims 2, 4-6, 50-60, 70, 71, and 74 are under final rejection, and are each appealed. Claims 75 and 76, though rejected in the final Office Action, were objected to in the Advisory Action after amendment by the Applicant, and have been indicated by the Examiner as including allowable subject matter. Claims 1, 3, 7-49, 61-69, and 72-73 were previously cancelled. Claims 2, 4-6, 50-60, 70, 71, and 74-76 are pending.

Status of Amendments after Final

The amendments to the claims made after final rejection have been entered, and are reflected in the Claims Appendix (Appendix A).

SUMMARY OF CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

In General

The present application is directed, in general, to an improved system allowing an embedded controller (230) and a host processor (214) to share access to modules (202, 204, 206, 208, 210, 224, 220, 216, 218, 212, 228, 215, etc.) in a computer system, as shown as part of chip 198 in Figure 9, below. The shared access system of the present invention enables exclusive, one-at-a-time access by a processor to a module and concurrent access by more than one processor to a module. An internal bus 258 with two power sources is used to allow continued access by one of the processors when one of the two power sources is not providing power. An example of a protocol that allows

an embedded controller to access more than one module is also described. *Abstract, page 28, line 17- page 29, line 14, and Figure 9, below.*

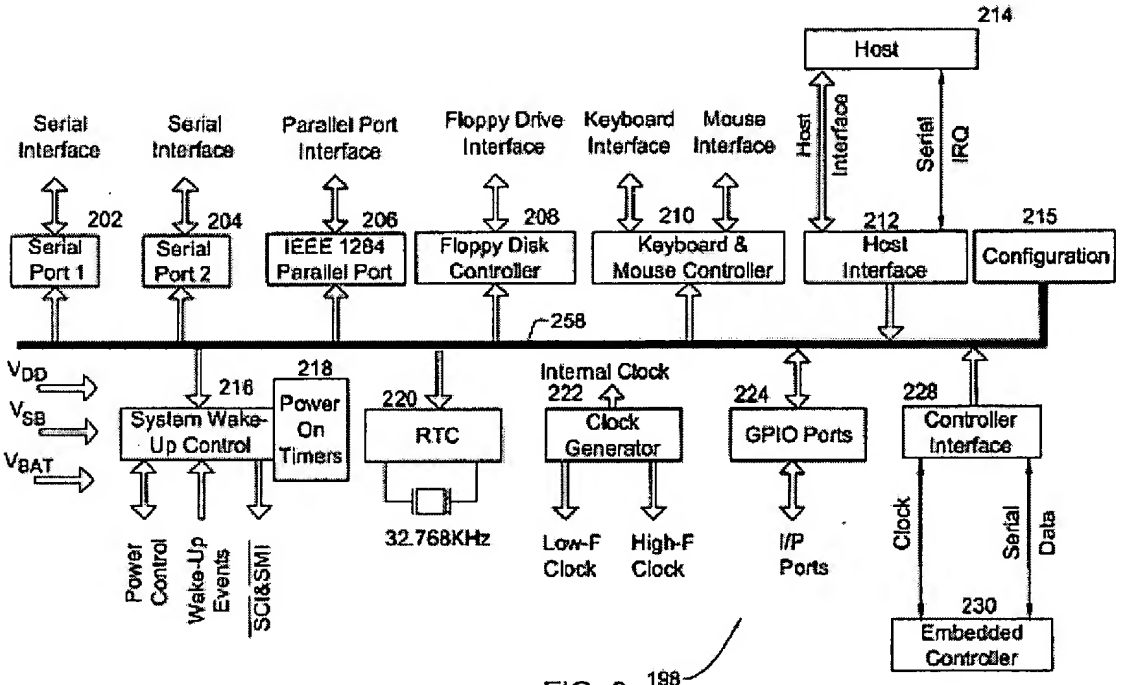

FIG. 9 198

Support for Independent Claims

Note that, per 37 CFR §41.37, only each of the independent claims are discussed in this section. In the arguments below, however, the dependent claims are also discussed and distinguished from the prior art. The discussion of the claims is for illustrative purposes, and is not intended to effect the scope of the claims.

Independent Claim 2 describes a system for allowing shared access by at least two processors including an embedded controller 230 and a host processor 214 to at least two modules (*e.g.*, modules (202, 204, 206, 208, 210, 224, 220, 216, 218, 212, 228, 215). *Page 14, lines 6-14 and Figure 9.*

The system of Claim 2 comprises a transaction control 256, shown in Figure 10, at right below. The embedded controller 230 is capable of providing an indication of which of the modules to access to the transaction control 256, and the host processor 214 is capable of providing an indication of which of the modules to access to the transaction control 256. *Page 14, lines 6-14, page 29, lines 20-24 and Figures 9 and 10.*

The system of Claim 2 also includes at least one access block bit 328 controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules. *Page 32, lines 8-14, page 51, lines 16-24, and Figure 13, next page.*

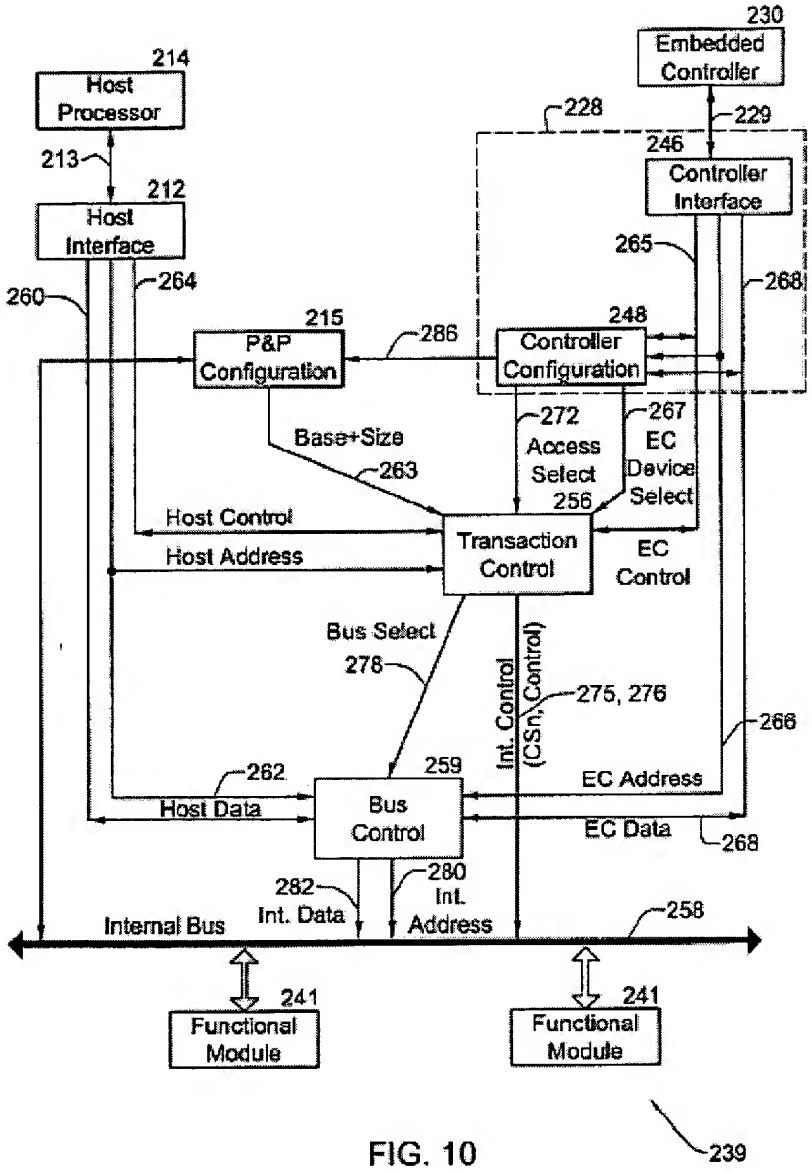

FIG. 10

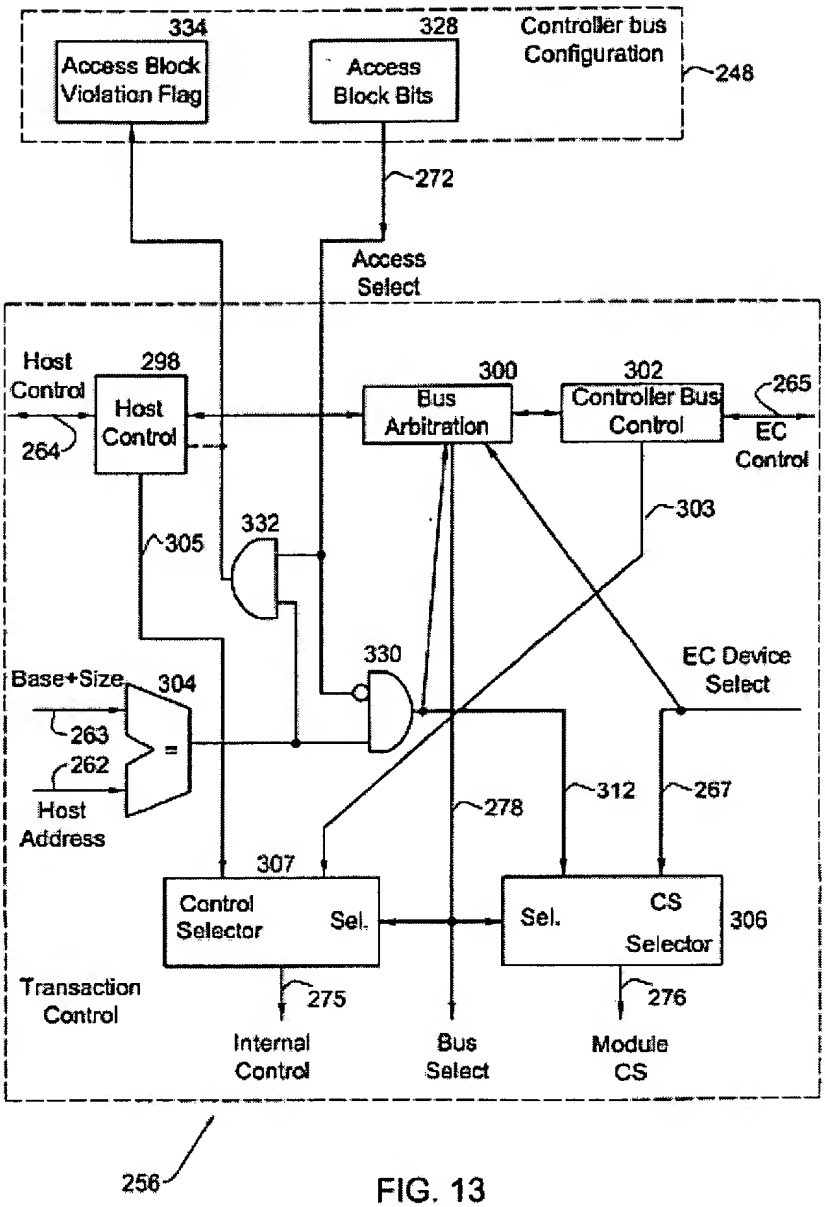

FIG. 13

Independent Claim 50 describes a method for allowing shared access to at least two modules by at least two processors including an embedded controller 230 and a host processor 214. *Page 17, lines 13-16, and Figure 9.*

The method includes receiving an indication from each of the processors of a module from among the at least two modules to access, arbitrating between the processors in favor of one of the processors, and accessing said module indicated by said one of the processors. *Page 17, lines 17-21,*

and Figure 9.

According to claim 50, arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, where the at least one access block bit is capable of blocking access by another of the processors to at least one of the modules, and capable of enabling at least one of modules. *Page 32, lines 8-14, page 51, lines 16-24, and Figure 13.*

Independent Claim 53 describes a method for allowing a processor comprising an embedded controller 230 to access at least two modules affiliated with a device. *Page 17, lines 22-24, and Figure 9.*

The method in Claim 53 includes indicating the device; indicating an access direction (read/write);
indicating one of the modules for accessing; indicating a location for accessing, within said indicated one of the modules; transferring data between said indicated location and the embedded controller. *Page 18, lines 1-5.*

According to claim 53, the method includes setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules. *Page 32, lines 8-14, page 51, lines 16-24, and Figure 13.*

Grounds of Rejection to be Reviewed on Appeal

1. **Are Claims 2, 4, 50-54, 70, and 71 anticipated by Lockwood (USP 5,339,443, "Lockwood")?**
2. **Are Claims 2, 4-6, and 50-60 obvious over Ku (USP 6,260,098, "Ku") in view of Glider *et al.* (USP 5,214,778, "Glider")?**
3. **Are Claims 2, 4-6, 50-60, 70, 71, and 74 obvious over Watanabe (US 2002/0129184, "Watanabe") in view of Glider?**

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

In Sections 6 and 7 of the July 26, 2005 Office Action, Claims 2, 4, 50-54, 70, and 71 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,339,443 to Lockwood ("Lockwood").

In Sections 8 and 9 of the July 26, 2005 Office Action, Claims 2, 4-6, and 50-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,260,098 to Ku ("Ku") in view of U.S. Patent No. 5,214,778 to Glider et al. ("Glider").

In Section 10 of the July 26, 2005 Office Action, Claims 2, 4-6, 50-60, 70, 71 and 74 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0129184 to Watanabe ("Watanabe") in view of Glider.

Legal Standards

The legal standards for an anticipation[1] rejection and an obviousness[2] rejection are referenced in the footnotes below.

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[1]The requirements to show anticipation are strict: "A party asserting that a patent claim is anticipated under 35 U.S.C. §102 "must demonstrate, among other things, identity of invention." *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 U.S.P.Q. 781, 789 (Fed Cir. 1983), *cert. denied*, 465 U.S. 1026 (1984), *overruled in part on another ground, SRI Int'l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1125, 227 U.S.P.Q. 577, 588-89 (Fed. Cir. 1985)*(in banc)*. Identity of invention is a question of fact, and one who seeks such a finding must show that each element of the claim in issue is found, either expressly or under principles of inherency, in a single prior art reference, or that the claimed invention was previously known or embodied in a single prior art device or practice. *Id.*

> *Minnesota Mining and Mfg. v. Johnson & Johnson Orthopaedics.*, 24 U.S.P.Q.2d 1321, 1326 (Fed.Cir. 1992)

[2]The Supreme Court has explained how to apply §103:

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined.
>
> *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459, 467 (1966).

Obviousness cannot be inferred from a combination of references without a showing that one of ordinary skill would have been motivated to combine those references:

> When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.
>
> *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 U.S.P.Q.2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 U.S.P.Q. 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 U.S.P.Q. 481 (Fed.Cir. 1984).

Analysis of Examiner's Rejection

The cited references are each briefly discussed in relevant part, and then the rejection of each claim is addressed separately under each ground of rejection.

Lockwood is drawn to a system for arbitrating multiprocessor accesses to shared resources, using access and grant bits to manage relative access priorities of the processors. As such, Lockwood shares some structural similarities with the instant application. However, Lockwood does not include several claimed elements and functions, as described in detail below, and certainly does not meet an anticipation standard.

Ku is drawn to a shared peripheral controller using multiple buses and a control unit to manage instructions sent to a peripheral by multiple processors. While Ku shares some structural similarities with the instant application, it does not include several claimed elements and functions, as described in detail below.

Watanabe is drawn to improving bus utilization using a bus arbiter. Watanabe uses a bus controller to arbitrate access requests from multiple processors in a multi-bus system. While Ku also shares some structural similarities with the instant application, it does not include several claimed elements and functions, as described in detail below.

Glider is drawn to resource management in a multiple-resource system, where the resources have various "availability states". Glider's structure and operation is relatively dissimilar to the instant application and the other cited art, and appears to be cited by the Examiner solely for its two sentences mentioning a "semaphore."

Ground of Rejection 1: Claims 2, 4, 50-54, 70, and 71 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,339,443 to Lockwood ("Lockwood").

Claim 2

Claim 2 requires, among other limitations: "A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules". This passage explicitly requires at least an embedded controller and a host processor, not taught by Lockwood. The passage of Lockwood cited by Examiner Mason states

> ...processors 12a-12n may be a mix of different well known processors that do not support read-modify-write operations in like manner or do not support read-modify-write operations at all. Particular examples of these processors 12a-12n include SPARC™ processors manufactured by Sun Microsystems, Inc. , Mountain View, Calif. , and i486™ processors manufactured by Intel, Inc. , Santa Clara, Calif. (SPARC™ . is a registered trademark of Sun Microsystems, Inc, and i486™ is a registered trademark of Intel, Inc.)

Examiner Mason includes a 1998 press release describing a "SPARCengine CompackPCi Family of Embedded-Board Computers." Lockwood refers to "SPARC processors", not "SPARCengine CompackPCi Embedded-Board Computers", and it is unclear from this press release exactly what an "Embedded-Board Computer" is. This press release, included in the Evidence Appendix, indicates that the "Embedded-Board Computer" will "initially be available with Sun's 270 MHz, 64-bit UltraSPARC™ microprocessor" (page 2 of 3). Nothing in this press release indicates that this is an embedded processor, although it describes some computer that, like the system in Lockwood, evidently includes some SPARC processor. Certainly nothing in Lockwood itself teaches or suggests anything about an embedded processor or a host processor, or how they might differ or work together.

Claim 2 also requires, among other limitations: "at least one access block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules". This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Lockwood.

Page 51, lines 7-12 of the specification as filed states:

> Enabling of a module typically implies that the module is activated (the internal clock is running); the resources of the module are assigned (for example, base address/size, interrupts, DMA); and/or the runtime registers of the module 45 are enabled for access.

Nothing in Lockwood in any way teaches or suggests that the "access grant bits" are in any way capable of enabling any shared resource, as that term is described in the specification. In

particular, Examiner Mason interprets the term "enable" according to the IEEE dictionary, not the specification, as a "command or condition that permits some specific condition to occur" or a "command or condition that permits some specific event to proceed." (Office Action, Page 2, Last paragraph). Examiner then asserts that an "access grant bit" of Lockwood is unset by one processor after that processor completes access to a shared resource, allowing other processors to access the shared resource. (Office Action, Page 2, Last paragraph - Page 3, First paragraph). Based on these particular definitions of the term "enable," the Examiner Mason asserts that unsetting the "access grant bit" of Lockwood enables access to the shared resource and therefore enables the shared resource. (Office Action, Page 3, First paragraph).

Even Examiner Mason's preferred definitions of the term "enable" fail to establish that Lockwood anticipates Claims 2 According to the definitions provided in the Office Action, the term "enable" refers to any "command or condition" that permits a specific "condition" or "event" to occur or proceed. Based on these definitions, the unsetting of the "access grant bit" by one processor in Lockwood does "enable" access to a shared resource by another processor. However, the unsetting of the "access grant bit" only enables "access" to the shared resource. The unsetting of the "access grant bit" does not actually enable the shared resource itself. For example, unsetting the "access grant bit" does not activate the shared resource.

This distinction is actually acknowledged in the Office Action. The Office Action specifically states that the unsetting of the "access grant bit" is a command or condition that "permits another processor to access the shared resource." (Office Action, Page 3, First paragraph). As a result, the Office Action expressly acknowledges that unsetting the "access block bit" only enables "access" to the shared resource rather than actually enabling the shared resource itself.

The setting and unsetting of the "access grant bit" in Lockwood only enables or disables "access" to a resource and does not actually enable or disable the resource itself.

Other dictionary definitions, known to those of skill in the art, are more consistent with the use of "enable" as in the specification. For example, the *IBM Dictionary of Computing* defines "enable" as "(1) To make functional. (2) In interactive communications, to load a start a subsystem. Contrast with disable." (Ninth Edition, October 1991). The McGraw-Hill Dictionary of Scientific and Technical Terms defines "enable" as "1. To authorize an activity which would otherwise be

suppressed, such as to write on a tape. 2. To turn on a computer system or a piece of equipment. To initiate the operation of a device or circuit by applying a trigger signal or pulse." (Sixth Edition, 2003). As can be seen, while "enable" can certainly be interpreted in different ways, specific definitions are consistent with the meaning ascribed in the specification, while others, such as those used by Examiner Mason, are inconsistent with the meaning ascribed in the specification.

The specification and claims as filed make a clear distinction between "enabling" a device – and even specifically describes what that term means in the context of the application – and granting or blocking access to a device. Examiner Mason's interpretation of these terms, contrary to their use in the application itself, ignores the plain language of the claims and specification, and therefore is not proper for an anticipation rejection.

For these reasons, the cited portion of Lockwood fails to anticipate the Applicants' invention as recited in Claim 2. Accordingly, Claim 2 should be allowed, and Examiner Mason's rejection should be reversed.

Claim 4

Claim 4 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 4 requires, among other limitations, "further comprising a bus extension ... wherein at least one of the modules is accessible via said bus extension ... and wherein said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors." Nothing in Lockwood appears to teach a bus extension, as claimed, and Examiner Mason has not even made a *prima facie* anticipation showing by alleging that any specific element in Lockwood corresponds to the claimed bus extension.

Claim 50

Claim 50 requires, among other limitations, "at least two processors including an embedded controller and a host processor." This passage explicitly requires at least an embedded controller and a host processor, not taught by Lockwood. Certainly nothing in Lockwood itself teaches or suggests anything about an embedded processor or a host processor, or how they might differ or work

together. The more detailed arguments with regard to embedded controllers not found in Lockwood, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 50 further requires, among other limitations, "arbitrating between the processors in favor of one of the processors, wherein arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, ...the at least one access block bit capable of enabling at least one of modules." This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Lockwood.

Nothing in Lockwood in any way teaches or suggests that the "access grant bits" are in any way capable of enabling any shared resource, as that term is described in the specification, as a part of an arbitration process as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 51

Claim 51 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 51 further requires, among other limitations, "blocking access by another of the processors to said module indicated by said one of the processors." This feature is not taught or suggested by Lockwood in the context of parent claim 50.

Claim 52

Claim 52 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 52 further requires, among other limitations, "aid indication from each of the processors is for a different module to access." This feature is not taught or suggested by Lockwood in the context of parent claim 50.

Claim 53

Claim 53 requires, among other limitations,"an embedded controller to access at least two modules affiliated with a device". This passage explicitly requires at least an embedded controller,

not taught by Lockwood. Certainly nothing in Lockwood itself teaches or suggests anything about an embedded controller. The more detailed arguments with regard to embedded controllers not found in Lockwood, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 53 further requires, among other limitations, "setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules". This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Lockwood.

Nothing in Lockwood in any way teaches or suggests that the "access grant bits" are in any way capable of "enabling" any shared resource, as that term is described in the specification, as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 54

Claim 54 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 54 further requires "wherein said indicated one of the modules is accessible via a bus extension". Nothing in Lockwood appears to teach a bus extension, as claimed, and Examiner Mason has not even made a *prima facie* anticipation showing by alleging that any specific element in Lockwood corresponds to the claimed bus extension.

Claim 70

Claim 70 depends from claim 4, so the arguments above with respect to claims 2 and 4 apply here, and these arguments are incorporated herein by reference.

Claim 70 requires, among other limitations, "wherein at least one of the modules comprises a memory accessible through the bus extension." Nothing in Lockwood appears to teach a bus extension, as claimed, nor that a memory is accessed through one, and Examiner Mason has not even made a *prima facie* anticipation showing by alleging that any specific elements in Lockwood

corresponds to the claimed bus extension and connected memory.

Claim 71

Claim 71 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference. Claim 71 requires, among other limitations, "wherein at least one of the modules comprises a memory accessible through a bus extension." Nothing in Lockwood appears to teach a bus extension, as claimed, nor that a memory is accessed through one, and Examiner Mason has not even made a *prima facie* anticipation showing by alleging that any specific elements in Lockwood corresponds to the claimed bus extension and connected memory.

Therefore, all claims should be allowed over Lockwood, and Examiner Mason's anticipation rejections should be reversed.

Ground of Rejection 2: Claims 2, 4-6, and 50-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,260,098 to Ku ("Ku") in view of U.S. Patent No. 5,214,778 to Glider et al. ("Glider").

These claims are allowable over this combination of references, as discussed below.

Claim 2

Claim 2 requires, among other limitations, "a transaction control, wherein the embedded controller is capable of providing an indication of which of the modules to access to the transaction control." The cited references do not appear to teach or suggest an embedded controller capable of providing an indication of which of modules to access to the transaction control, alone or in combination.

Examiner Mason notes correctly that Ku's service processor 620 is described as an embedded controller, and so corresponds to the claimed embedded controller, and indicates that Ku's CPU 602 corresponds to the claimed host processor. In order to reconstruct the limitation of claim 2, however, the Examiner then suggests that shared peripheral controller 100 - not service processor 620 - is

"capable of providing an indication of which of the modules to access said transaction control." Applicants respectfully submit that the Examiner's own citations not only show that Ku does not teach the required claim limitation, but also show that Ku teaches away from the required claim limitation. The passage cited by Examiner Mason reads, in its entirety:

> In the preferred embodiment, shared peripheral controller 100 is configured similarly with respect to operations received via secondary bus 108. More specifically, control unit 114 is preferably designed to detect a first segment of a second operation issued by a second processor that is coupled to secondary bus 108 and destined for the first shared peripheral on shared bus 112. Upon detecting the second operation's first segment, control unit 114 is configured to buffer the second operation's first segment in a secondary bus first register 130 accessible to control unit 114. The second operation's first segment is buffered in secondary bus first register 130 until the second operation's second segment is detected, at which time control unit 114 is configured to issue the first and second segments of the second operation to the first shared peripheral via shared bus 112 in consecutive cycles of shared bus 112 thereby eliminating the possibility of issuing an incorrect operation over shared bus 112 that might otherwise be caused by activity from primary bus 104 that occurs intermediate between the second operation's first and second segments.
>
> In embodiments designed for use with more than one shared peripheral, shared peripheral controller 100 includes additional buffer registers. In the depicted embodiment, a second set of buffer registers is indicated in phantom by primary bus second register 122 and secondary bus second register 132. This second set of registers is associated with a second shared peripheral that is coupled to shared

peripheral controller 100 via shared bus 112. (*Ku, col5, lines 34-61*)

As may be readily seen, nothing in this passage teaches that service processor 620 does or is capable of anything, much less that it is capable of providing an indication of which of the modules to access to the transaction control. As Glider does not contain a teaching or suggestion corresponding to the claims, either, this obviousness rejection must fail.

Examiner Mason also concedes that Ku fails to disclose "the system and method, where the system includes at least one block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, and where the at least one access block bit is capable of enabling at least one of the modules." Applicants agree. Applicants further submit that Ku contains no disclosure or suggestion of why such requirements might be necessary or desirable.

Nonetheless, Examiner Mason suggests that the Glider reference discloses a system that "includes at least one access block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules". Examiner Mason cites Glider's col. 5, lines 33-40, which read:

> 3. Semaphore
>
> The semaphore is a variable which is set by whatever portion of the system is using the resource to prevent anyone else from using the resource. The semaphore indicates simply that the resource is in use, while the availability state gives further information on the type of use.

While the teaching of "preventing anyone else from using" is, of course, functionally the same as the claimed "blocking access", it is clear that this passage in no way teaches that Glider's semaphore is implemented as "at least one access block bit controlled by one of the processors", as required by claim 2.

Further, and significantly, this passage at no point teaches that the semaphore " is capable of enabling at least one of the modules", as claimed. This feature is not taught or suggested by Ku or Glider, alone or in combination. As page 51, lines 7-12 of the specification as filed states:

> Enabling of a module typically implies that the module is activated

(the internal clock is running); the resources of the module are assigned (for example, base address/size, interrupts, DMA); and/or the runtime registers of the module 45 are enabled for access.

Nothing in Ku, Glider, or any combination of them in any way teaches or suggests that the "access grant bits" are in any way capable of enabling any shared resource, as that term is described in the specification, and so this claim should be allowed over these references. The more detailed discussion regarding "enabling", made above with respect to the anticipation rejection of claim 2, is relevant here and hereby incorporated by reference.

Further, even if all claim limitations were found in a combination of Ku and Glider, these references cannot be properly combined, as discussed more fully below under "Motivation to Combine or Modify."

Applicants respectfully request allowance of Claim 2 and reversal of Examiner Mason's rejections.

Claim 4

Claim 4 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 4 requires, among other limitations, "further comprising a bus extension ... wherein at least one of the modules is accessible via said bus extension ... and wherein said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors." Nothing in Ku or Glider, or any combination of them, appears to teach a bus extension, as claimed. Examiner Mason does reference Ku's "shared bus 112", but there is no teaching in Ku that this shared bus 112 is a bus extension, as claimed.

Claim 5

Claim 5 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 5 further requires "wherein said transaction control is capable of providing an indication of at least one of the modules for access by one of the processors." While Examiner Mason refers to Ku's shared peripheral controller 100 as the claimed transaction control, nothing in Ku, or any other cited art, teaches or suggests that this element functions as described with relation to all other elements of this and the parent claims.

Claim 6

Claim 6 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 6 further requires " wherein at least one of the modules is part of an input/output chip." Examiner Mason references Ku's col. 7, lines 20-59, but neither this passage, nor any other part of Ku or the cited art, teaches or suggests an input/output chip, particularly in the context of the parent claim.

Claim 50

Claim 50 requires, among other limitations, "arbitrating between the processors in favor of one of the processors, wherein arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, ...the at least one access block bit capable of enabling at least one of modules." This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Ku, Glider, or any combination of them. Nothing in Ku or Glider in any way teaches or suggests that the Glider's semaphores are in any way capable of enabling any shared resource, as that term is described in the specification, as a part of an arbitration process as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 51

Claim 51 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 51 further requires, among other limitations, "blocking access by another of the processors to said module indicated by said one of the processors." This feature is not taught or suggested by Ku, Glider, or any combination of them in the context of parent claim 50.

Claim 52

Claim 52 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 52 further requires, among other limitations, "aid indication from each of the processors is for a different module to access." This feature is not taught or suggested by Ku, Glider, or any combination of them in the context of parent claim 50.

Claim 53

Claim 53 requires, among other limitations, "setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules". " This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Ku, Glider, or any combination of them. Nothing in Ku or Glider in any way teaches or suggests that the Glider's semaphores are in any way capable of enabling any shared resource, as that term is described in the specification, as a part of an arbitration process as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, is relevant here and is herein incorporated by reference.

Claim 54

Claim 54 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 54 further requires "wherein said indicated one of the modules is accessible via a bus

extension". Nothing in Ku or Glider, or any combination of them, appears to teach a bus extension, as claimed. Examiner Mason does reference Ku's "shared bus 112", but there is no teaching in Ku that this shared bus 112 is a bus extension, as claimed.

Claim 55

Claim 55 depends from claim 54, so the arguments above with respect to claims 53 and 54 apply here, and these arguments are incorporated herein by reference.

Claim 55 further requires "wherein said step of indicating one of the modules for accessing includes the step of: indicating one of at least one chip select corresponding to said bus extension for accessing." Nothing in Ku or Glider, or any combination of them, teaches or suggests this featre. As described above, no bus extension is taught or suggested by the art, and further, no chip select corresponding to the bus extension is taught or suggested by any art of reference. Examiner Mason does reference Ku's col. 5, lines 2-61, but this passage does not appear to include any such teaching.

Claim 56

Claim 56 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 56 further requires "said indicated one of the modules is part of an input/output chip." Examiner Mason references Ku's col. 7, lines 20-59, but neither this passage, nor any other part of Ku or the cited art, teaches or suggests an input/output chip, particularly in the context of the parent claim

Claim 57

Claim 57 depends from claim 56, so the arguments above with respect to claims 53 and 56 apply here, and these arguments are incorporated herein by reference.

Claim 57 further requires " wherein said step of indicating one of the modules for accessing includes the step of: indicating a logical device number." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or

suggested by Ku or Glider.

Claim 58

Claim 58 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 58 further requires:"wherein said step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said modules, the method further comprising the step of: waiting for a freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Examiner Mason references Ku's col. 5, lines 2-61, but neither this passage, nor any other part of Ku or the cited art, teaches or suggests waiting for a freeing up of an internal bus before transferring the indication of a location for accessing onto the internal bus, as claimed.

Claim 59

Claim 58 depends from claim 58, so the arguments above with respect to claims 53 and 58 apply here, and these arguments are incorporated herein by reference.

Claim 59 further requires "wherein said internal bus is occupied by a transaction originating from the other processor prior to said freeing up". Nothing in Ku, Glider, or any combination of them teaches or suggests this feature in the context of the parent claims. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or suggested by Ku or Glider.

Claim 60

Claim 60 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 60 requires "the embedded controller waiting for receipt of data from said indicated location prior to initiating a subsequent access." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or suggested by Ku or Glider.

Therefore, all claims should be allowed over the combination of Ku and Glider, and Examiner Mason's obviousness rejections should be reversed.

Ground of Rejection 3: Claims 2, 4-6, 50-60, 70, 71 and 74 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0129184 to Watanabe ("Watanabe") in view of Glider.

These claims are allowable over this combination of references, as discussed below.

Claim 2

Claim 2 requires, among other limitations, "A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules, comprising: a transaction control, wherein the embedded controller is capable of providing an indication of which of the modules to access to the transaction control."

The cited references do not appear to teach or suggest an embedded controller capable of providing an indication of which of modules to access to the transaction control, alone or in combination. In fact, neither Watanabe, nor Glider, nor any combination of them, teaches, suggests – or even mentions – an embedded controller at all. Examiner Mason cites Watanabe's second processor/DMA controller 160, but at no point is this in any way taught or suggested to be an embedded controller, as required by the claims. As the cited art does not contain a teaching or suggestion corresponding to the claims, this obviousness rejection must fail.

Examiner Mason also concedes that Watanabe fails to disclose "the system and method, where the system includes at least one block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, and where the at least one access block bit is capable of enabling at least one of the modules." Applicants agree. Applicants further submit that Watanabe contains no disclosure or suggestion of why such requirements might be necessary or desirable.

Nonetheless, Examiner Mason suggests that the Glider reference discloses a system that "includes at least one access block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules". Examiner Mason cites Glider's col. 5, lines 33-40, which read:

> 3. Semaphore
>
> The semaphore is a variable which is set by whatever portion of the system is using the resource to prevent anyone else from using the resource. The semaphore indicates simply that the resource is in use, while the availability state gives further information on the type of use.

While the teaching of "preventing anyone else from using" is, of course, functionally the same as the claimed "blocking access", it is clear that this passage in no way teaches that Glider's semaphore is implemented as "at least one access block bit controlled by one of the processors", as required by claim 2.

Further, and significantly, this passage at no point teaches that the semaphore "is capable of enabling at least one of the modules", as claimed. This feature is not taught or suggested by Watanabe or Glider, alone or in combination. As page 51, lines 7-12 of the specification as filed states:

> Enabling of a module typically implies that the module is activated (the internal clock is running); the resources of the module are assigned (for example, base address/size, interrupts, DMA); and/or the runtime registers of the module 45 are enabled for access.

Nothing in Watanabe, Glider, or any combination of them in any way teaches or suggests that the "access grant bits" are in any way capable of enabling any shared resource, as that term is described in the specification, and so this claim should be allowed over these references. The more detailed discussion regarding "enabling", made above with respect to the anticipation rejection of claim 2, is relevant here and hereby incorporated by reference.

Further, even if all claim limitations were found in a combination of Watanabe and Glider, these references cannot be properly combined, as discussed more fully below under "Motivation to Combine or Modify."

Applicants respectfully allowance of Claim 2 and reversal of Examiner Mason's rejections.

Claim 4

Claim 4 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 4 requires, among other limitations, "further comprising a bus extension ... wherein at least one of the modules is accessible via said bus extension ... and wherein said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors." Nothing in Watanbe or Glider, or any combination of them, appears to teach a bus extension, as claimed. Examiner Mason does reference Watanabe's "sub bus 165", but there is no teaching in Watanabe that this sub bus 165 is a bus extension, as claimed.

Claim 5

Claim 5 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 5 further requires "wherein said transaction control is capable of providing an indication of at least one of the modules for access by one of the processors." While Examiner Mason refers to Watanabe's bus controller 150 as the claimed transaction control, nothing in Watanaba, or any other cited art, teaches or suggests that this element functions as described with relation to all other elements of this and the parent claims.

Claim 6

Claim 6 depends from Claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 6 further requires " wherein at least one of the modules is part of an input/output chip." Examiner Mason references Watanabe's paragraph 0015, but neither this passage, nor any other part of Watanabe or the cited art, teaches or suggests that one of the modules is an input/output chip, particularly in the context of the parent claim. In fact, this paragraph of Watanabe suggests that one of the processors is an input/output device.

Claim 50

Claim 50 requires, among other limitations, "arbitrating between the processors in favor of one of the processors, wherein arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, ...the at least one access block bit capable of enabling at least one of modules." This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Watanabe, Glider, or any combination of them. Nothing in Watanabe or Glider in any way teaches or suggests that the Glider's semaphores are in any way capable of enabling any shared resource, as that term is described in the specification, as a part of an arbitration process as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, are relevant here and is herein incorporated by reference.

Claim 51

Claim 51 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 51 further requires, among other limitations, "blocking access by another of the processors to said module indicated by said one of the processors." This feature is not taught or suggested by Watanabe, Glider, or any combination of them in the context of parent claim 50.

Claim 52

Claim 52 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 52 further requires, among other limitations, "aid indication from each of the processors is for a different module to access." This feature is not taught or suggested by Watanabe, Glider, or any combination of them in the context of parent claim 50.

Claim 53

Claim 53 requires, among other limitations, "setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit

is capable of enabling at least one of the modules". " This passage requires an access block bit that also is "capable of enabling" at least one of the modules. This feature is not taught or suggested by Watanabe, Glider, or any combination of them. Nothing in Watanabe or Glider in any way teaches or suggests that the Glider's semaphores are in any way capable of enabling any shared resource, as that term is described in the specification, as a part of an arbitration process as claimed. The more detailed arguments with regard to enabling modules, above with regard to claim 2, are relevant here and is herein incorporated by reference.

Claim 54

Claim 54 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 54 further requires "wherein said indicated one of the modules is accessible via a bus extension". Nothing in Watanbe or Glider, or any combination of them, appears to teach a bus extension, as claimed. Examiner Mason does reference Watanabe's "sub bus 165", but there is no teaching in Watanabe that this sub bus 165 is a bus extension, as claimed.

Claim 55

Claim 55 depends from claim 54, so the arguments above with respect to claims 53 and 54 apply here, and these arguments are incorporated herein by reference.

Claim 55 further requires "wherein said step of indicating one of the modules for accessing includes the step of: indicating one of at least one chip select corresponding to said bus extension for accessing." Nothing in Watanabe or Glider, or any combination of them, teaches or suggests this feature. As described above, no bus extension is taught or suggested by the art, and further, no chip select corresponding to the bus extension is taught or suggested by any art of reference. Examiner Mason does make a peculiar reference Watanabe's peripheral device 170, but this element does not appear to relate at all to the claim limitation.

Claim 56

Claim 56 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 56 further requires "said indicated one of the modules is part of an input/output chip." Examiner Mason references Watanabe's paragraph 15, but neither this passage, nor any other part of Watanabe or the cited art, teaches or suggests that one of the modules is an input/output chip, particularly in the context of the parent claim. In fact, this paragraph of Watanabe suggests that one of the processors is an input/output device.

Claim 57

Claim 57 depends from claim 56, so the arguments above with respect to claims 53 and 56 apply here, and these arguments are incorporated herein by reference.

Claim 57 further requires " wherein said step of indicating one of the modules for accessing includes the step of: indicating a logical device number." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or suggested by Watanabe or Glider.

Claim 58

Claim 58 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 58 further requires:"wherein said step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said modules, the method further comprising the step of: waiting for a freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Examiner Mason references Watanabe's paragraphs 0018-0019, but neither this passage, nor any other part of Watanabe or the cited art, teaches or suggests waiting for a freeing up of an internal bus before transferring the indication of a location for accessing onto the internal bus, as claimed.

Claim 59

Claim 58 depends from claim 58, so the arguments above with respect to claims 53 and 58 apply here, and these arguments are incorporated herein by reference.

Claim 59 further requires "wherein said internal bus is occupied by a transaction originating from the other processor prior to said freeing up". Nothing in Watanabe, Glider, or any combination of them teaches or suggests this feature in the context of the parent claims. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or suggested by Watanabe or Glider.

Claim 60

Claim 60 depends from claim 53, so the arguments above with respect to claim 53 apply here, and these arguments are incorporated herein by reference.

Claim 60 requires "the embedded controller waiting for receipt of data from said indicated location prior to initiating a subsequent access." This feature, in the context of the parent claims, is not taught or suggested by the art of reference. Further, Examiner Mason has not made even a *prima facie* rejection, as she has not alleged at all where this feature might be taught or suggested by Watanabe or Glider.

Claim 70

Claim 70 depends from claim 4, so the arguments above with respect to claims 2 and 4 apply here, and these arguments are incorporated herein by reference.

Claim 70 further requires "at least one of the modules comprises a memory accessible through the bus extension". Nothing in Watanabe or Glider, or a combination of them, appears to teach a bus extension, as claimed, nor that a memory is accessed through one, particularly in the context of claim 4.

Claim 71

Claim 71 depends from claim 50, so the arguments above with respect to claim 50 apply here, and these arguments are incorporated herein by reference.

Claim 71 further requires "at least one of the modules comprises a memory accessible through the bus extension". Nothing in Watanabe or Glider, or a combination of them, appears to teach a bus extension, as claimed, nor that a memory is accessed through one, particularly in the context of claim 50.

Claim 74

Claim 74 depends from claim 2, so the arguments above with respect to claim 2 apply here, and these arguments are incorporated herein by reference.

Claim 74 further requires "wherein the transaction control is further capable of allowing concurrent access by the processors to at least one of: one or more of the modules, and one or more sub-modules within at least one of the modules". This feature does not appear to be taught or suggested by Watanabe or Glider, or a combination of them, particularly in the context of claim 2.

Therefore, all claims should be allowed over the combination of Watanabe and Glider, and Examiner Mason's obviousness rejections should be reversed.

Motivation to Combine or Modify[3]

Examiner Mason includes conclusory "motivation" statements as a part of her final Office Action. Examiner Mason's stated motivation for combining either Ku or Watanabe with Glider is

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[3]Where an obviousness rejection is based on a combination of references, the Examiner must show that one of ordinary skill would have been motivated to combine those references. *See In re Nilssen*, 7 USPQ2d 1500 (Fed.Cir. 1988); *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed.Cir. 1987); *ACS Hospital Systems v. Montefiore Hospital*, 220 USPQ 929 (Fed.Cir. 1984).

"When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination." *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 USPQ2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 USPQ 481 (Fed.Cir. 1984).

"While *[a reference]* may be capable of being modified to run the way *[the applicant's]* apparatus is claimed, there must be a suggestion or motivation in the reference to do so. See In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) ("The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."). *In re Mills,* 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed.Cir. 1990).

"to allow for real time sharing of resources without disrupting services provided by the system" (pages 10 and 14 of the 7/26/05 Office Action). Examiner Mason makes reference to Glider's col. 1, lines 38-42, which reads, "[w]hat is needed, therefore, is a computing system that manages access to the resources so that the operation of the fault management subsystems do not cause any interruption of the services provided by the operational subsystems."

According to Examiner Mason, then, both Ku and Watanabe must have some unsolved problem with "disrupting services provided by the system", so they look to Glider to "allow for real time sharing of resources." This is not the case, so this stated motivation to combine fails.

Ku is drawn to a shared peripheral controller having multiple bus interfaces, and managing instructions sent to peripherals using a buffer technique. Nothing in Ku teaches or suggests that there is some unresolved issue with "real time sharing of resources", since Ku addresses peripheral sharing issues using a shared bus and a buffer. " There is, therefore, no motivation at all for Ku to look to Glider for any help with a problem related to "disrupting services provided by the system", since Ku solves the very problem with which it is concerned. Furthermore, there is no teaching or suggestion, or any allegation by Examiner Mason, that Glider's "semaphore" would even be operable in Ku's system or would provide any advantages in such a system.

Watanabe is drawn to a bus arbiter for managing bus utilization in a multi-bus system. The only "resources" that Watanabe is concerned with sharing are the buses themselves, and Watanabe's teachings provide "efficient bus accesses in a multi-bus system." There is, therefore, no motivation at all for Watanabe to look to Glider for any help with a problem related to "disrupting services provided by the system", since Watanabe solves the very problem with which it is concerned. Furthermore, there is no teaching or suggestion, or any allegation by Examiner Mason, that Glider's "semaphore" would even be operable in Watanabe's system or would provide any advantages in such a system.

Grouping of Claims

The claims on appeal do not stand or fall together, as may be seen from the arguments set forth below. Each claim has been argued separately under a separate subheading, and each claim should be considered separately. While the applicant recognizes that a formal statement regarding the grouping of claims is no longer required, each claim should be considered separately; or at the very least each claim which is argued separately in the preceding sections of this brief should be considered separately. Argument: The fact that the claims use different formulations (as detailed above) and/or have been argued separately, shows that, if their patentability is not considered separately, any adverse decision would show that the limitations of some claims had been unfairly ignored.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,
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Date: Dec. 15, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ohad Falik, et al.
Serial No.:	09/810,746
Filed:	March 16, 2001
For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

APPENDIX A -

Claims Appendix

1. (Cancelled).

2. (Previously Presented) A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules, comprising:

a transaction control, wherein the embedded controller is capable of providing an indication of which of the modules to access to the transaction control, and wherein the host processor is capable of providing an indication of which of the modules to access to the transaction control; and

at least one access block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules.

3. (Cancelled).

4. (Previously Presented) The system of claim 2, further comprising a bus extension;

wherein at least one of the modules is accessible via said bus extension;

wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor;

wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller; and

wherein said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors.

5. (Previously Presented) The system of claim 2, wherein said transaction control is capable of providing an indication of at least one of the modules for access by one of the processors.

6. (Previously Presented) The system of claim 2, wherein at least one of the modules is part of an input/output chip.

Claims 7-49 (Cancelled).

50. (Previously Presented) A method for allowing shared access to at least two modules by at least two processors including an embedded controller and a host processor, comprising the steps of:

receiving an indication from each of the processors of a module from among the at least two modules to access;

arbitrating between the processors in favor of one of the processors, wherein arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, the at least one access block bit capable of blocking access by another of the processors to at least one of the modules, the at least one access block bit capable of enabling at least one of modules; and

accessing said module indicated by said one of the processors.

51. (Previously Presented) The method of claim 50, further comprising the step of:

blocking access by another of the processors to said module indicated by said one of the processors.

52. (Previously Presented) The method of claim 50, wherein said indication from each of the processors is for a different module to access.

53. (Previously Presented) A method for allowing a processor comprising an embedded controller to access at least two modules affiliated with a device, comprising the steps of:

indicating the device;

indicating an access direction (read/write);

indicating one of the modules for accessing;

indicating a location for accessing, within said indicated one of the modules;

transferring data between said indicated location and the embedded controller; and

setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules.

54. (Previously Presented) The method of claim 53, wherein said indicated one of the modules is accessible via a bus extension.

55. (Previously Presented) The method of claim 54, wherein said step of indicating one of the modules for accessing includes the step of:

indicating one of at least one chip select corresponding to said bus extension for accessing.

56. (Previously Presented) The method of claim 53, wherein said indicated one of the modules is part of an input/output chip.

57. (Previously Presented) The method of claim 56, wherein said step of indicating one of the modules for accessing includes the step of:

indicating a logical device number.

58. (Previously Presented) The method of claim 53, wherein said step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said modules, the method further comprising the step of:

waiting for a freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus.

59. (Previously Presented) The method of claim 58, wherein said internal bus is occupied by a transaction originating from the other processor prior to said freeing up.

60. (Previously Presented) The method of claim 53, further comprising the step of:

the embedded controller waiting for receipt of data from said indicated location prior to initiating a subsequent access.

Claims 61-69 (Cancelled).

70. (Previously Presented) The system of Claim 4, wherein at least one of the modules comprises a memory accessible through the bus extension.

71. (Previously Presented) The method of Claim 50, wherein at least one of the modules comprises a memory accessible through a bus extension.

72. (Cancelled).

73. (Cancelled).

74. (Previously Presented) The system of Claim 2, wherein the transaction control is further capable of allowing concurrent access by the processors to at least one of: one or more of the modules, and one or more sub-modules within at least one of the modules.

75. (Previously Presented) The system of Claim 2, further comprising:

at least one disable bit controlled by one of the processors, wherein the at least one disable bit is capable of disabling at least one of the modules even if the at least one access block bit is set to enable the at least one module; and

at least one tri-state bit controlled by one of the processors, wherein the at least one tri-state bit is capable of disabling an output of at least one of the modules even if the at least one access block bit is set to enable the at least one module.

76. (Previously Presented) The system of Claim 2, wherein the at least one access block bit is capable of enabling at least one of the modules by activating the at least one module.

DOCKET NO. P04931 (NATI15-04931) **PATENT**
CUSTOMER NO. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ohad Falik, et al.
Serial No.:	09/810,746
Filed:	March 16, 2001
For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

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P.O. Box 1450
Alexandria, VA 22313-1450

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Date: 12/15/05

Nancy J. Lambert
Mailer

Date: Dec. 15, 2005

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PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/810,746
Filing Date	March 16, 2001
First Named Inventor	Ohad Falik
Examiner Name	Donna K. Mason
Art Unit	2111
Attorney Docket No.	P04931 (NATI15-04931)

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Davis Munck, P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief filing fee	$500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 39,308	Telephone 972-628-3600
Name (Print/Type)	William A. Munck		Date Dec. 15, 2005

DUPLICATE

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/810,746
Filing Date	March 16, 2001
First Named Inventor	Ohad Falik
Examiner Name	Donna K. Mason
Art Unit	2111
Attorney Docket No.	P04931 (NATI15-04931)

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Davis Munck, P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief filing fee	$500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 39,308	Telephone 972-628-3600
Name (Print/Type)	William A. Munck		Date Dec. 15, 2005

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ohad Falik, et al.
Serial No.:	09/810,746
Filed:	March 16, 2001
For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

APPENDIX B -
Copy of Formal Drawings

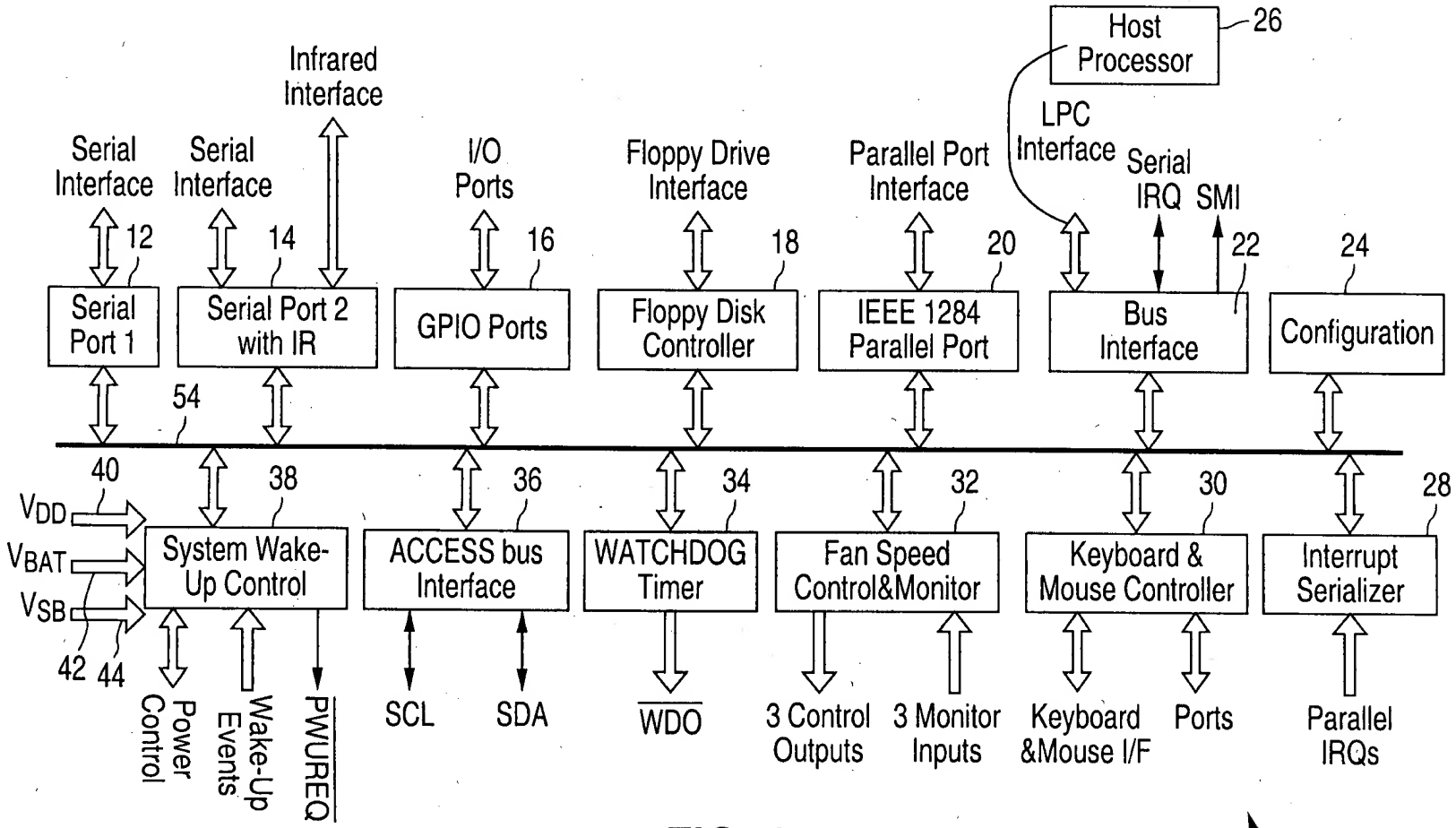

FIG. 1
(PRIOR ART)

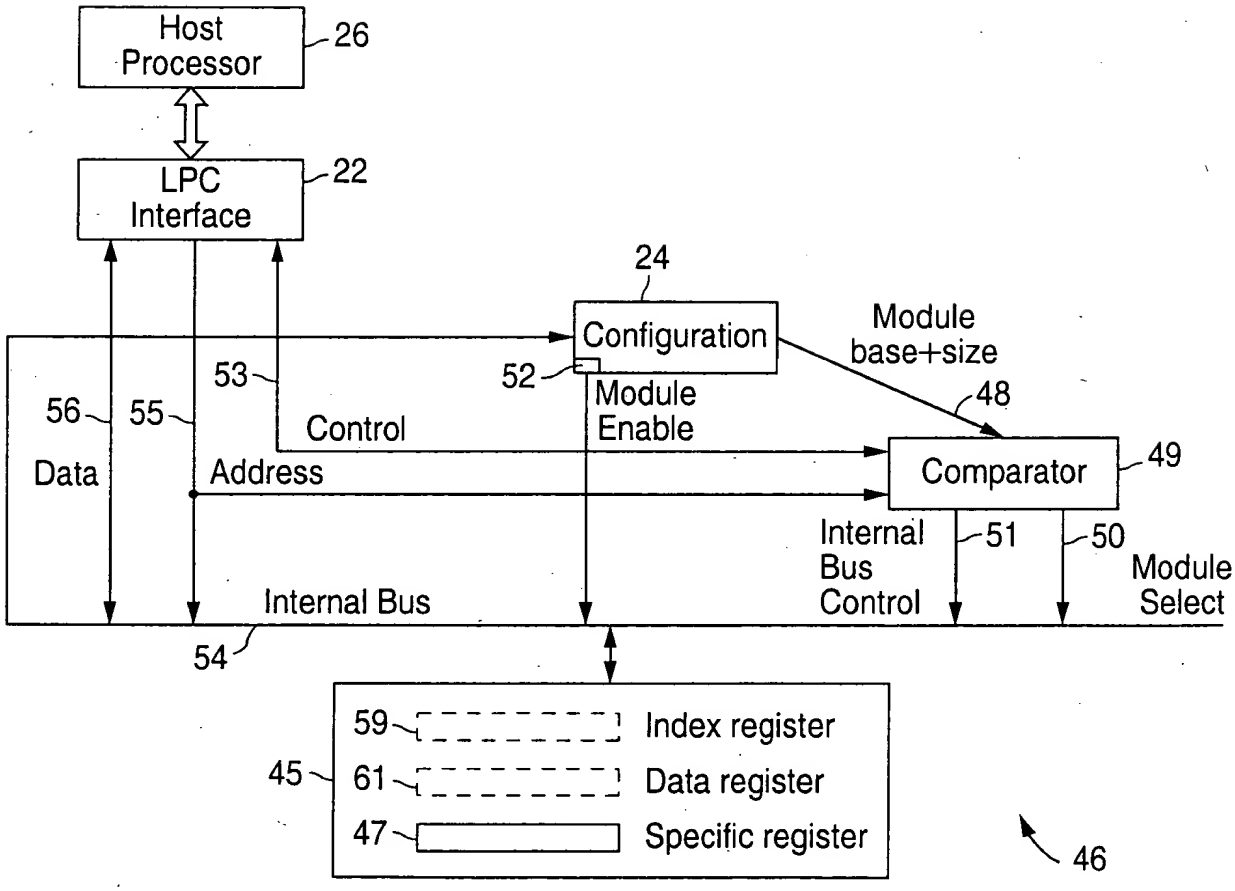

FIG. 2
(PRIOR ART)

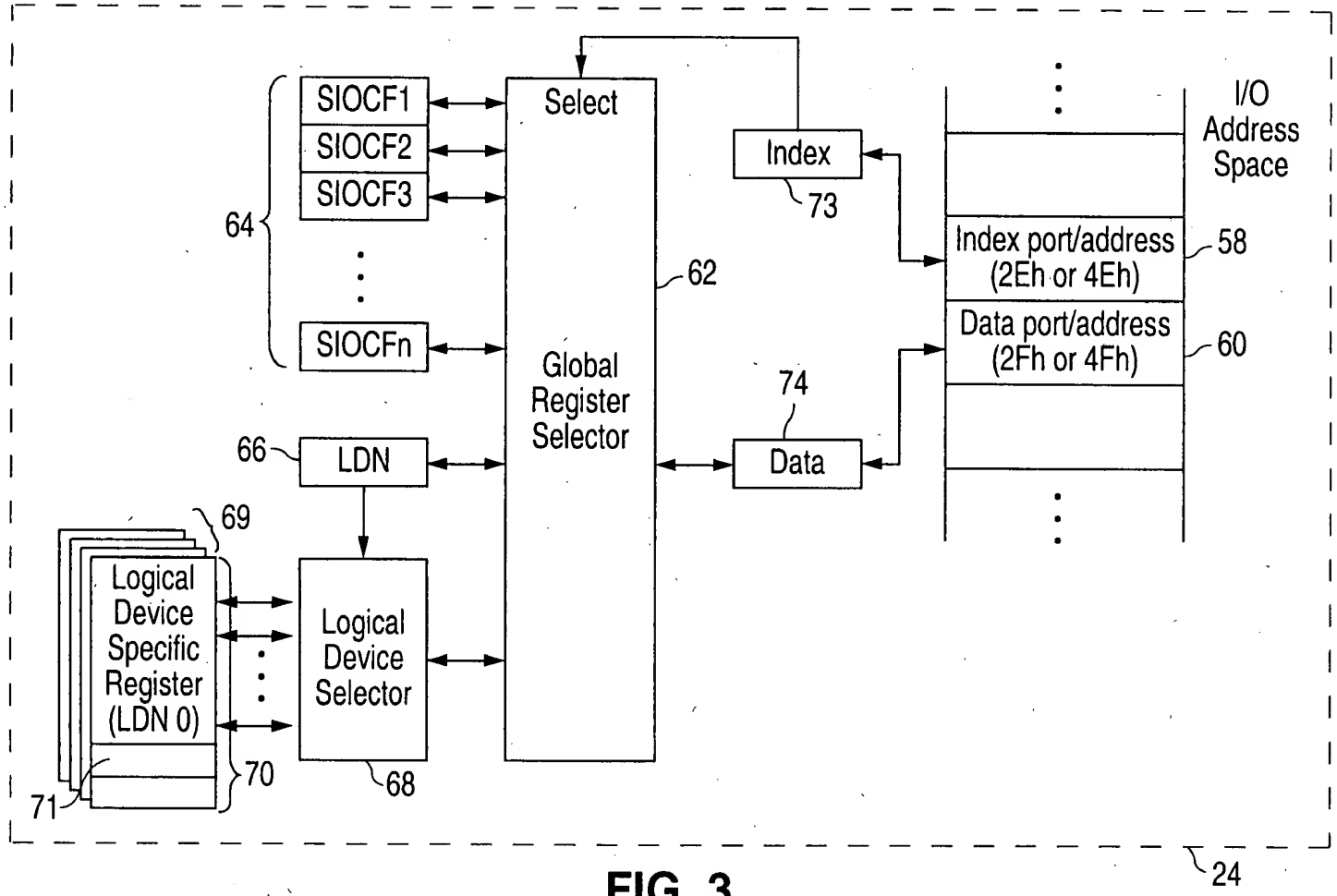

FIG. 3
(PRIOR ART)

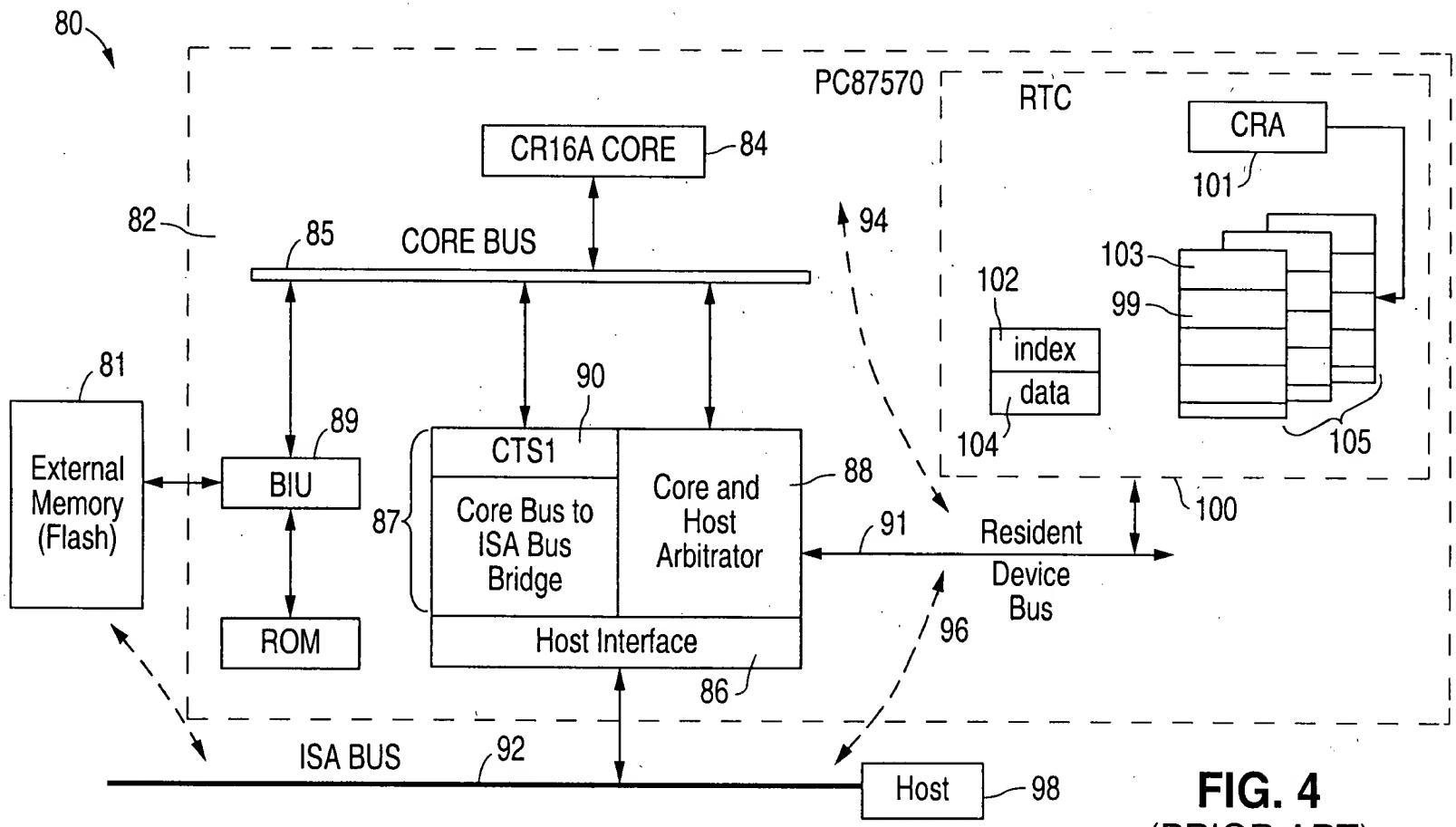

FIG. 4
(PRIOR ART)

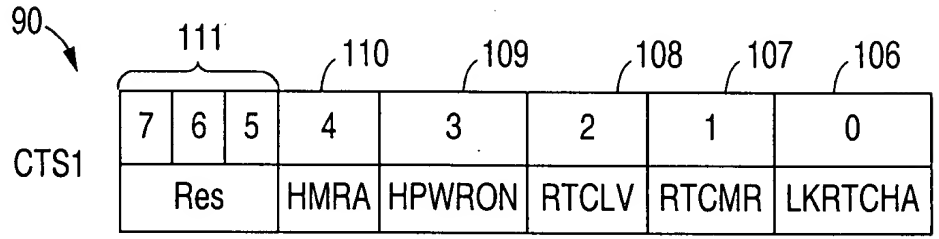

FIG. 5
(PRIOR ART)

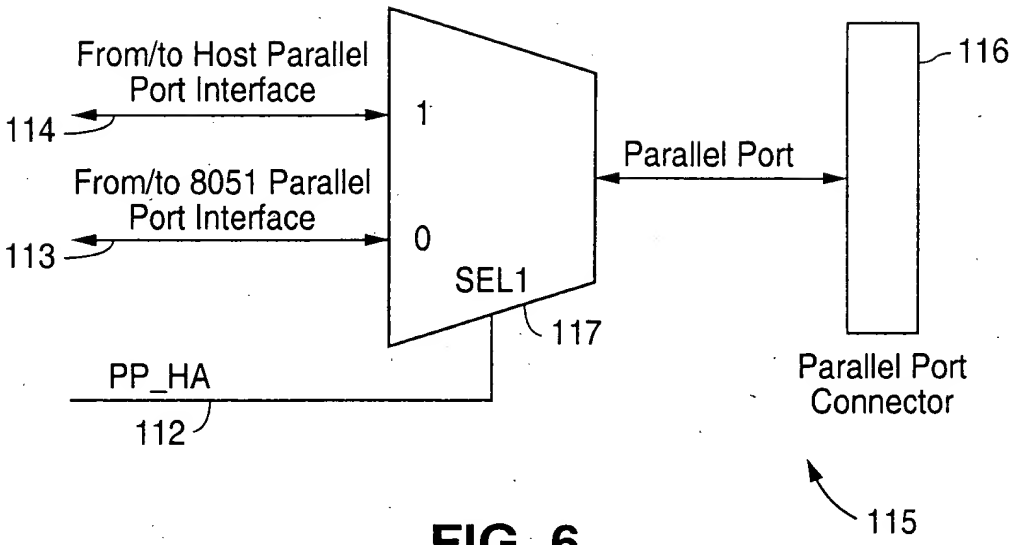

FIG. 6
(PRIOR ART)

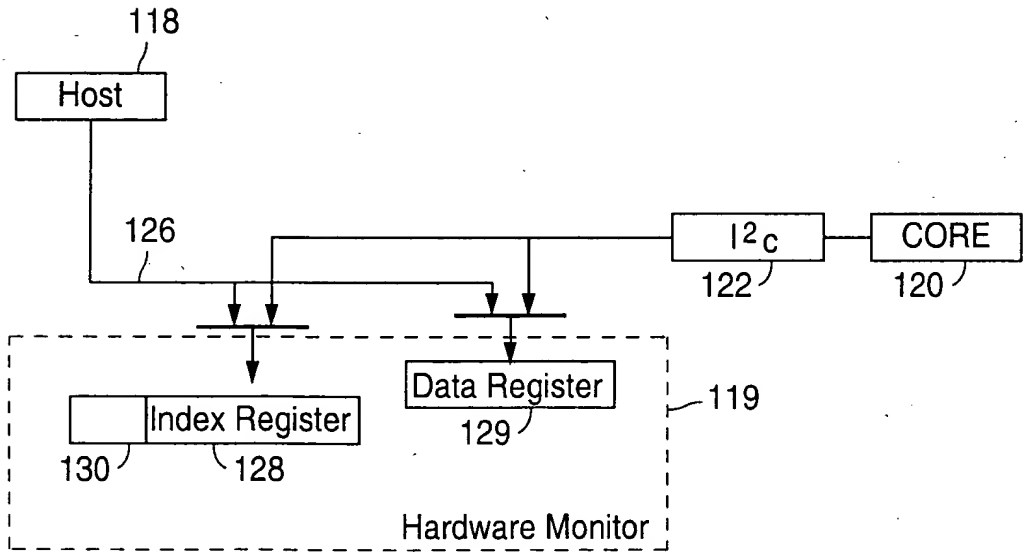

FIG. 7
(PRIOR ART)

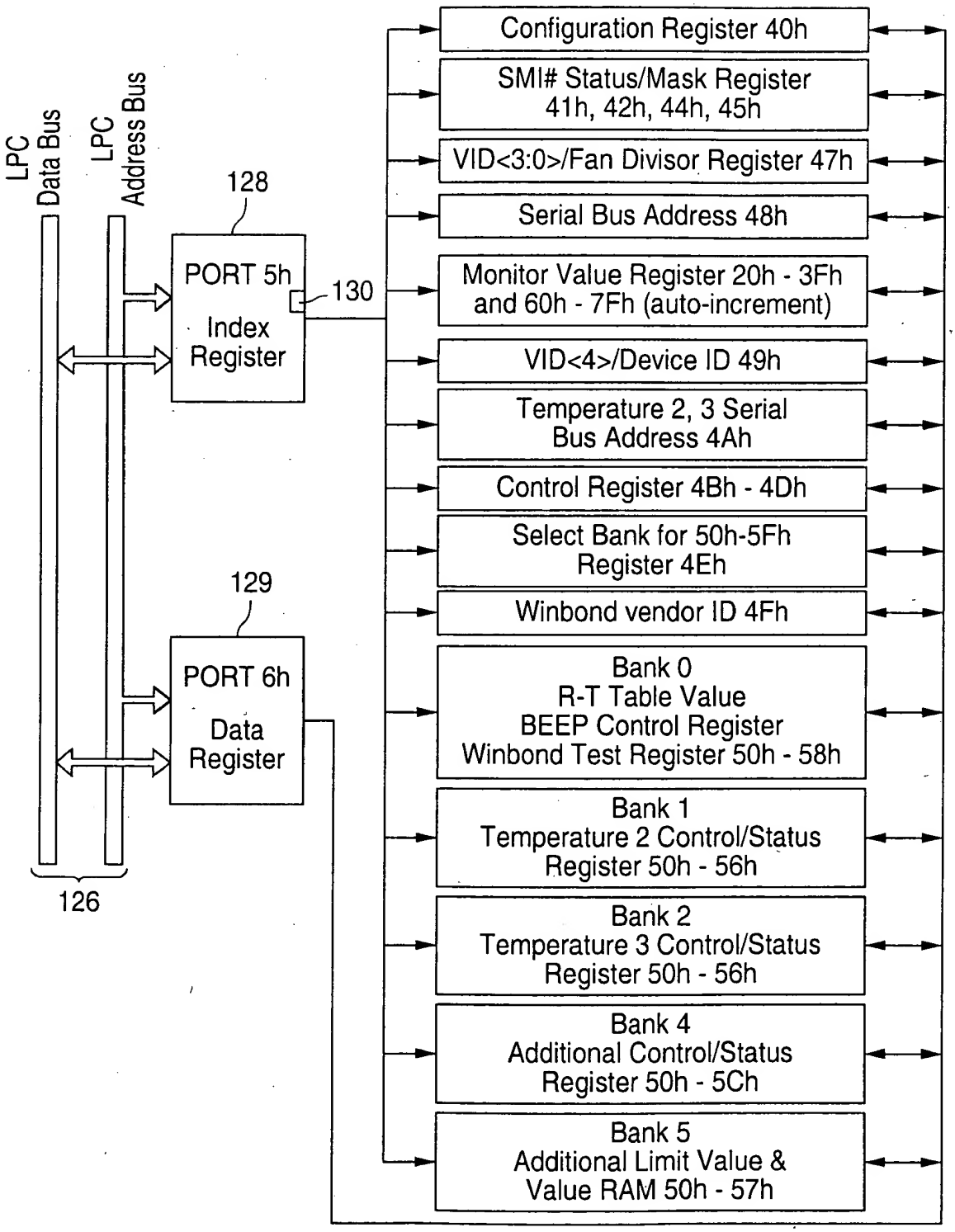

FIG. 8
(PRIOR ART)

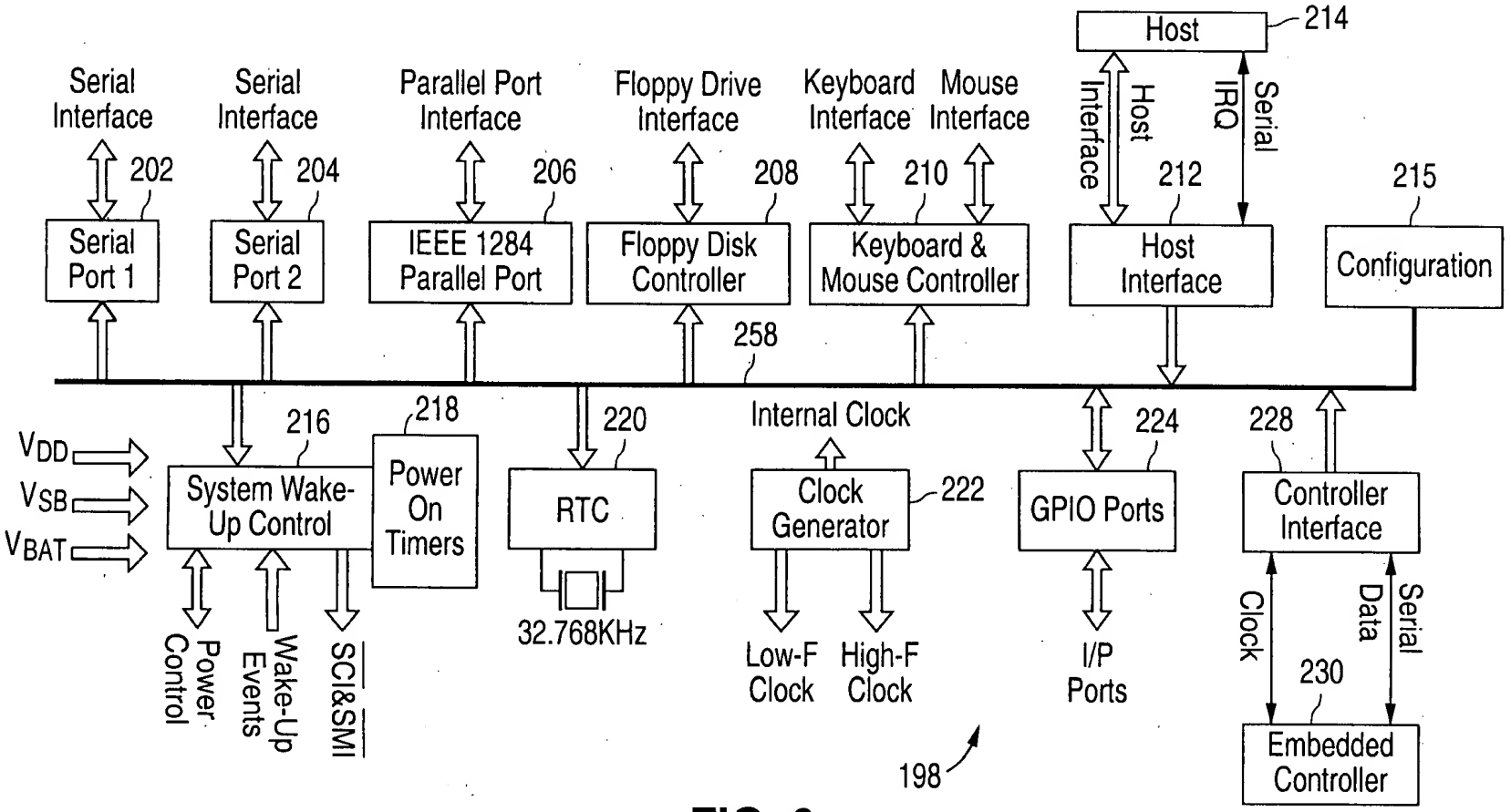
Host
214
Serial Interface
Serial Interface
Parallel Port Interface
Floppy Drive Interface
Keyboard Interface
Mouse Interface
Host Interface
Host
IRQ
Serial
202
204
206
208
210
212
215
Serial Port 1
Serial Port 2
IEEE 1284 Parallel Port
Floppy Disk Controller
Keyboard & Mouse Controller
Host Interface
Configuration
258
V_{DD}
V_{SB}
V_{BAT}
216
218
220
Internal Clock
224
228
System Wake-Up Control
Power On Timers
RTC
Clock Generator
222
GPIO Ports
Controller Interface
Power Control
Wake-Up Events
SCI&SMI
32.768KHz
Low-F Clock
High-F Clock
I/P Ports
Clock
Data
Serial
230
Embedded Controller
198

FIG. 9

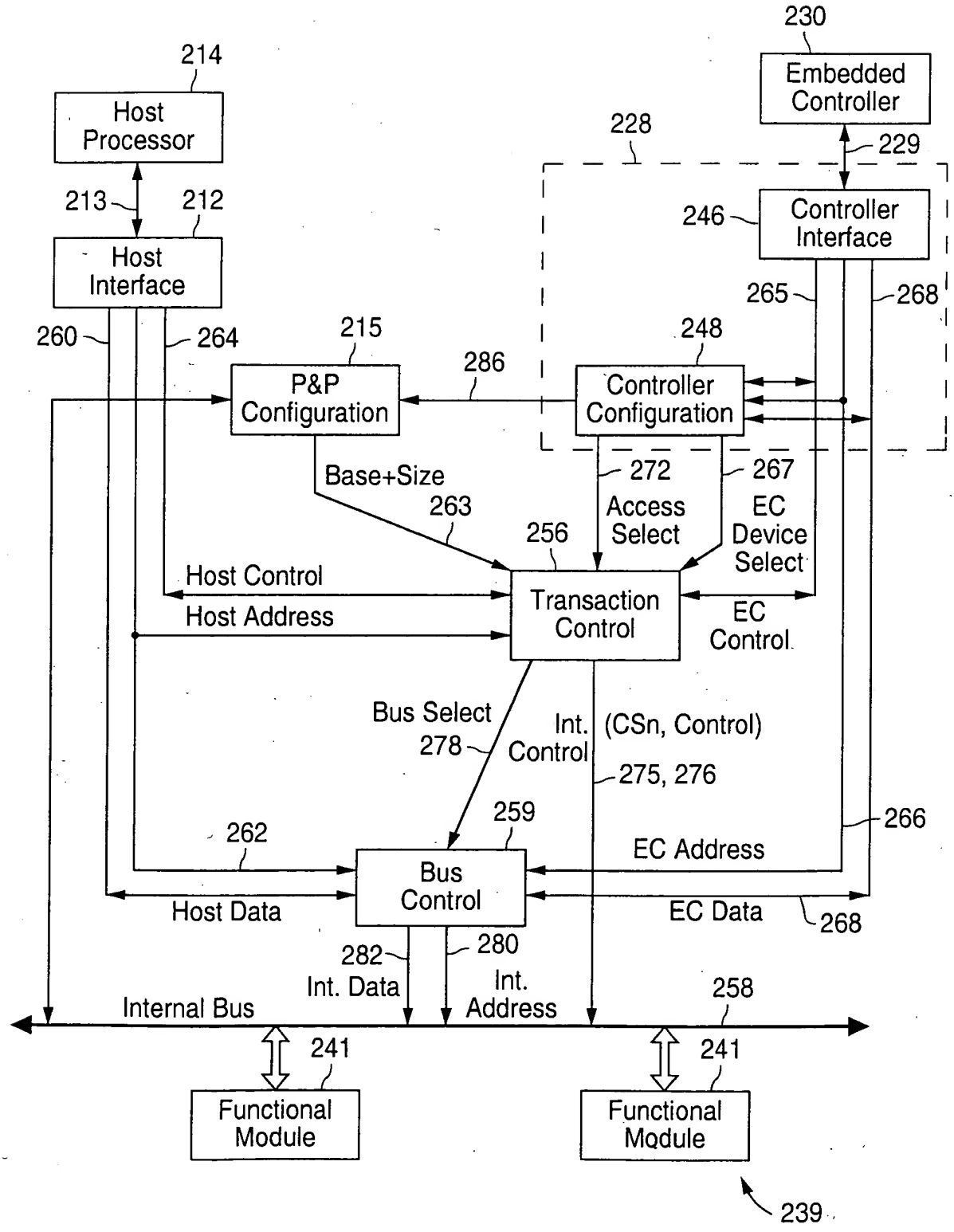
230
Embedded Controller
214
Host Processor
228
229
213
212
246
Controller Interface
Host Interface
265
268
260
264
215
248
286
P&P Configuration
Controller Configuration
Base+Size
272
267
263
Access Select
EC Device Select
256
Host Control
Transaction Control
Host Address
EC Control
Bus Select
278
Int. Control
(CSn, Control)
275, 276
259
266
262
EC Address
Bus Control
Host Data
EC Data
268
282
280
Int. Data
Int. Address
258
Internal Bus
241
241
Functional Module
Functional Module
239

FIG. 10

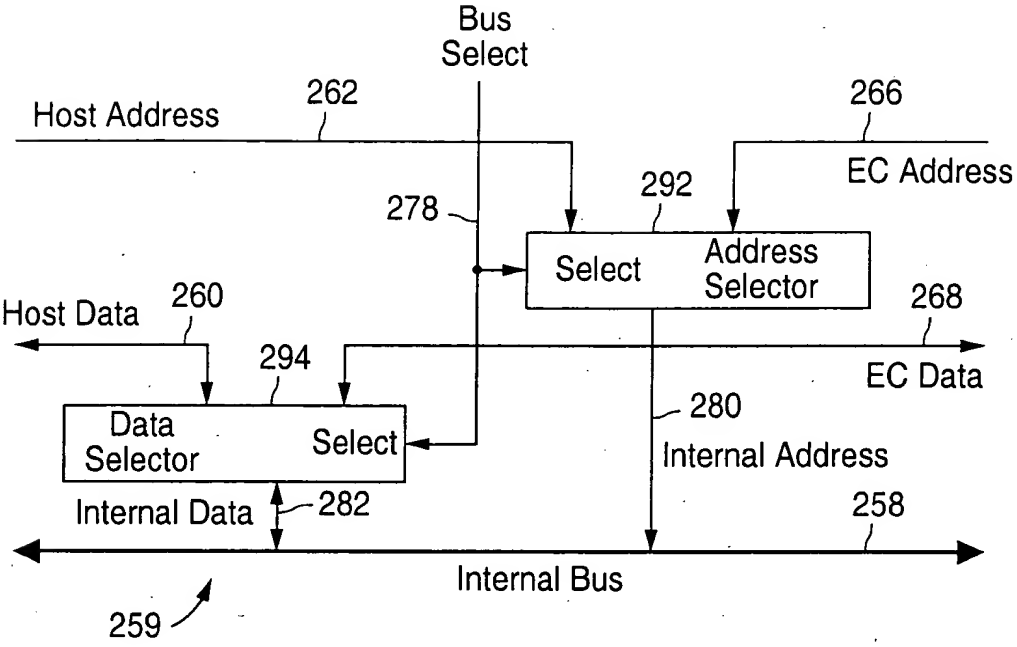
Bus
Select
Host Address
262
266
EC Address
292
278
Select
Address
Selector
Host Data
260
268
294
EC Data
Data
Selector
Select
280
Internal Address
Internal Data
282
258
Internal Bus
259

FIG. 11

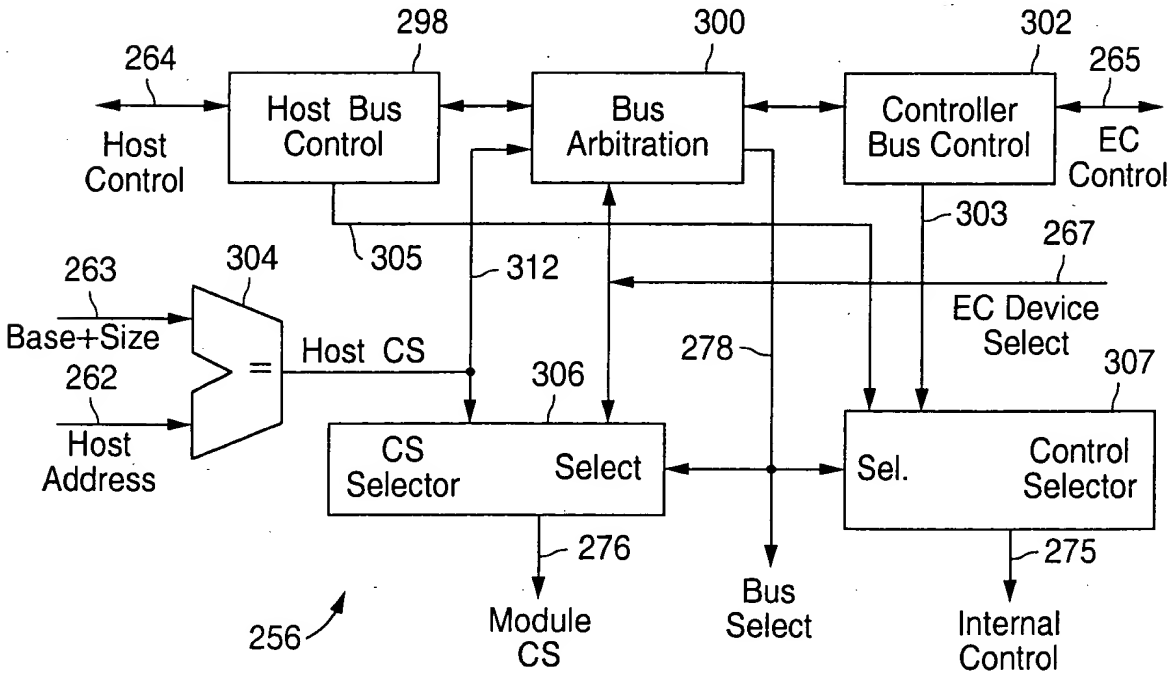
298
300
302
264
265
Host Bus
Control
Bus
Arbitration
Controller
Bus Control
Host
Control
EC
Control
303
267
305
312
263
304
EC Device
Select
Base+Size
Host CS
278
307
262
306
Host
Address
CS
Selector
Select
Sel.
Control
Selector
276
275
256
Module
CS
Bus
Select
Internal
Control

FIG. 12

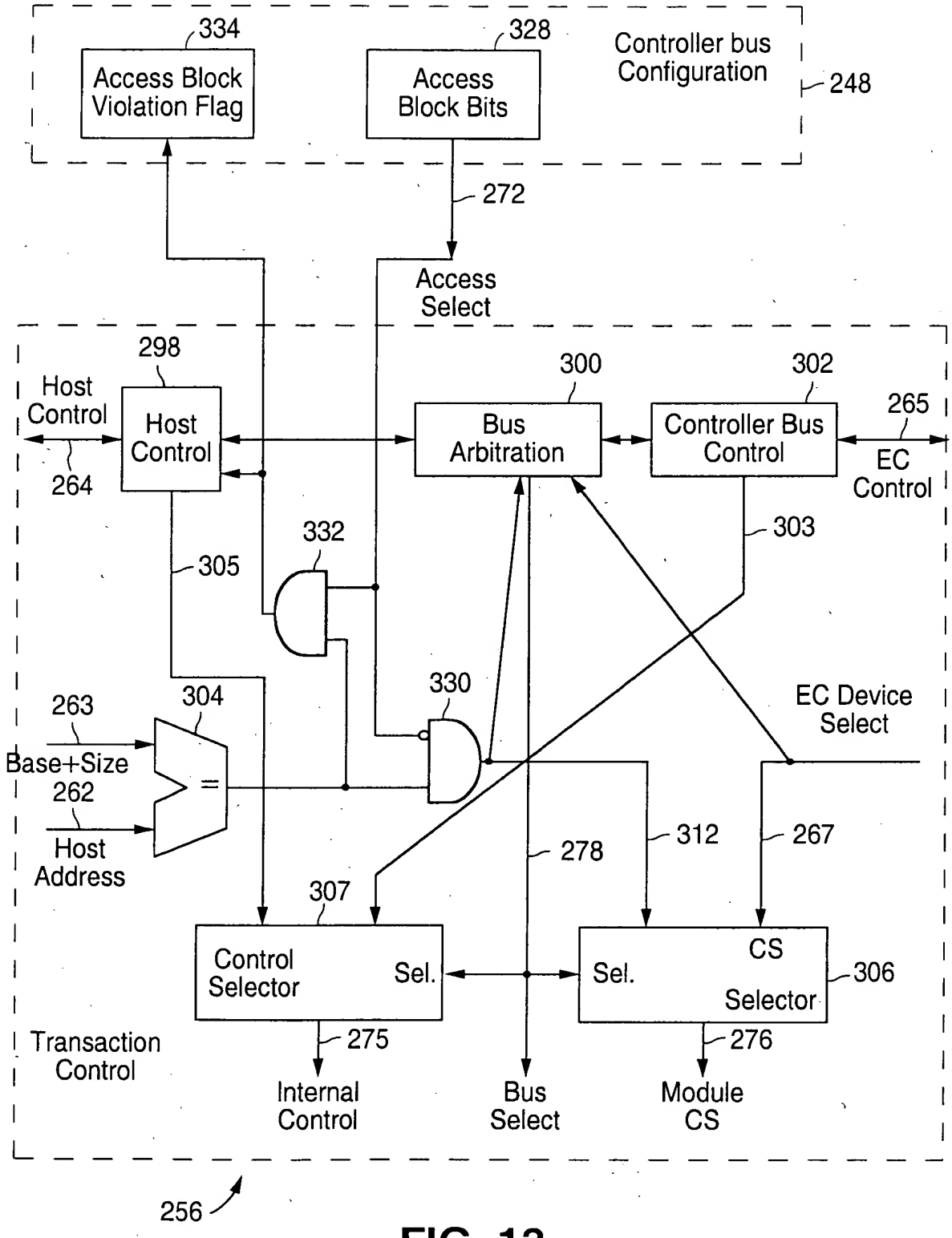
334
Access Block Violation Flag
328
Access Block Bits
Controller bus Configuration
248
272
Access Select
298
Host Control
Host Control
264
300
Bus Arbitration
302
Controller Bus Control
265
EC Control
303
305
332
330
304
263
Base+Size
262
Host Address
EC Device Select
278
312
267
307
Control Selector
Sel.
Sel.
CS Selector
306
Transaction Control
275
276
Internal Control
Bus Select
Module CS
256

FIG. 13

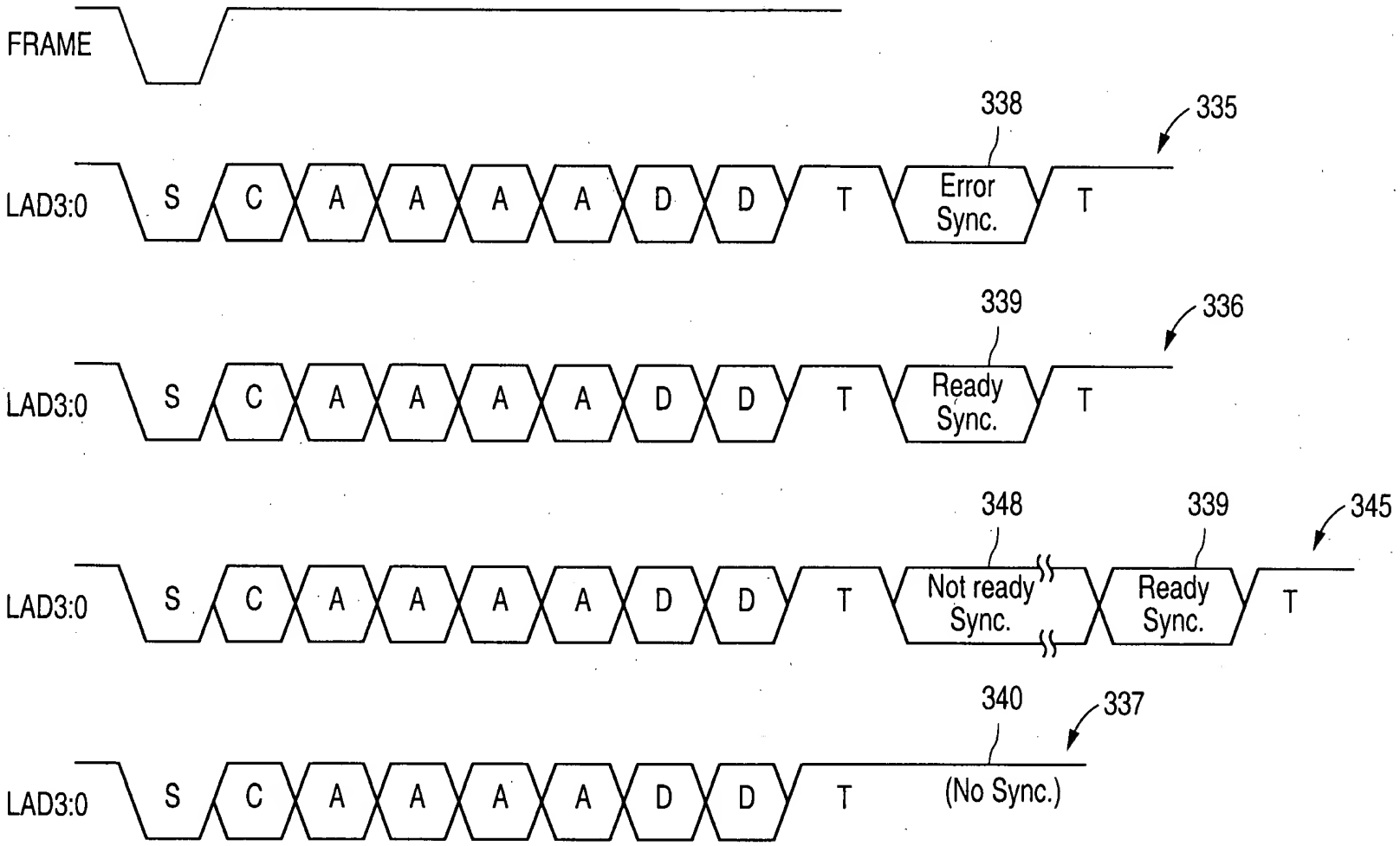

FIG. 14A

FIG. 14B

FIG. 14C

FIG. 14D

S = Start T = TAR

C = Cycle Type A = Address D = Data

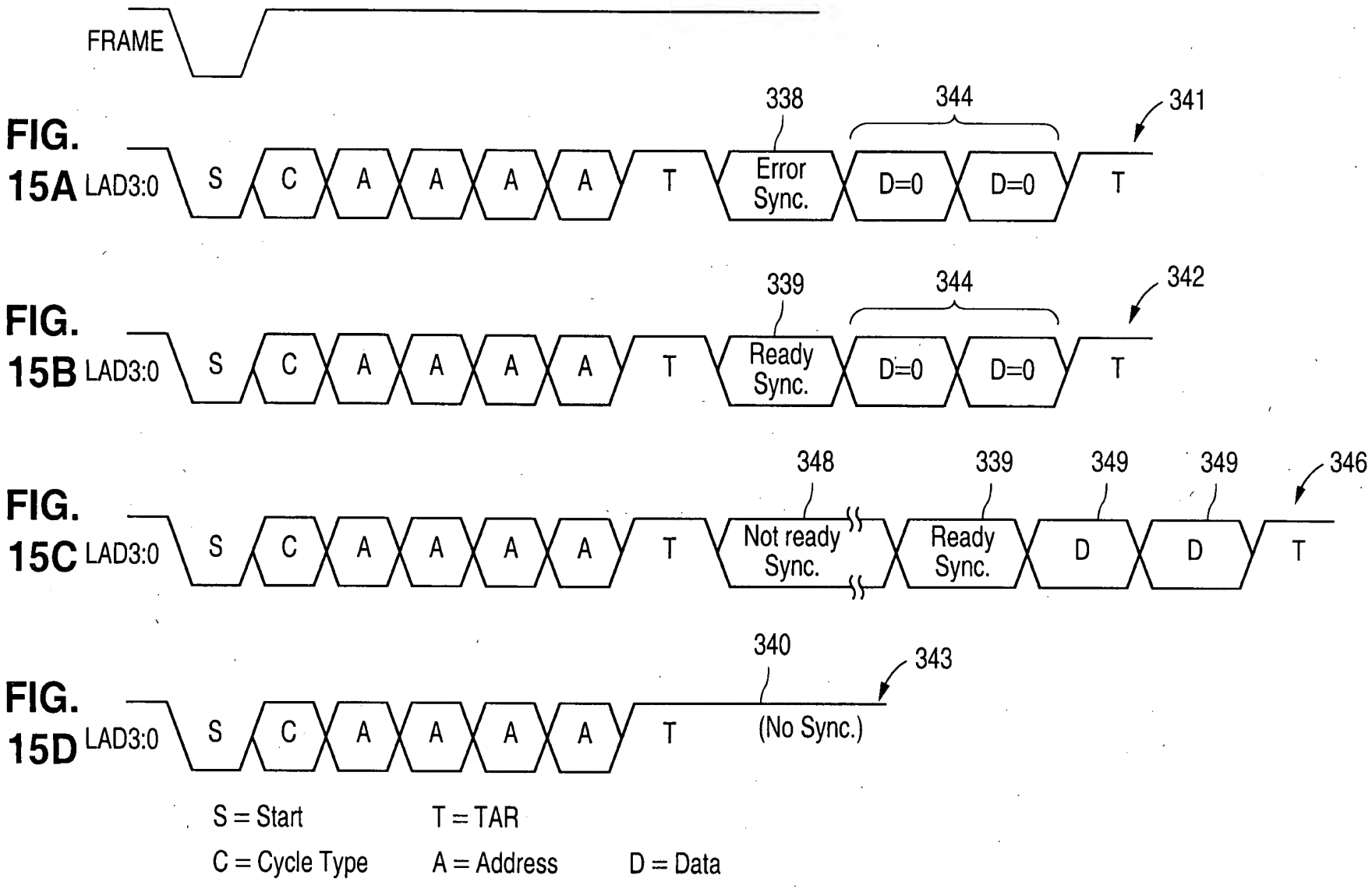

FIG. 15A

FIG. 15B

FIG. 15C

FIG. 15D

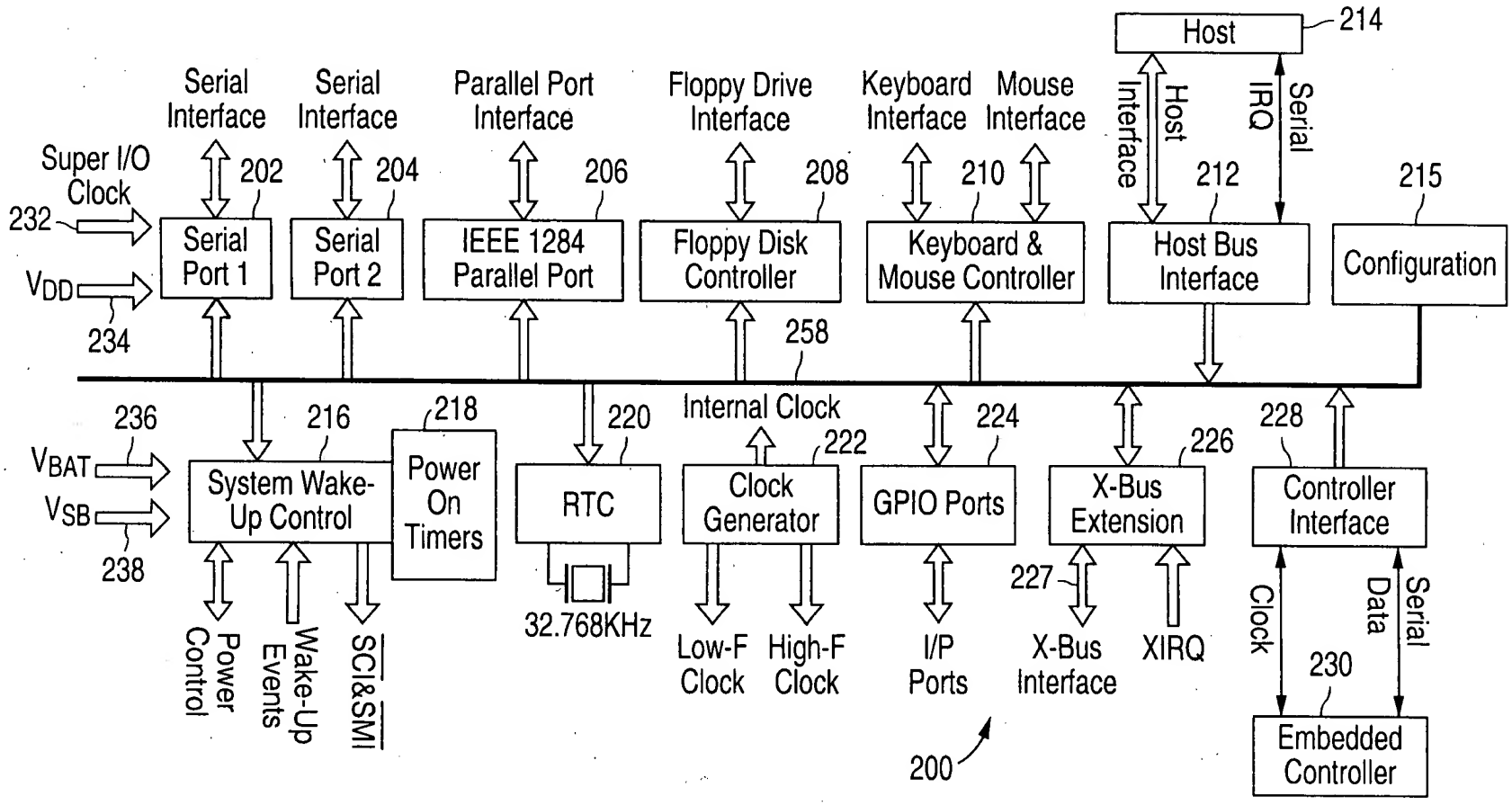
Host
214
Serial Interface
Serial Interface
Parallel Port Interface
Floppy Drive Interface
Keyboard Interface
Mouse Interface
Host Interface
Host IRQ
Serial
Super I/O Clock
232
202
204
206
208
210
212
215
Serial Port 1
Serial Port 2
IEEE 1284 Parallel Port
Floppy Disk Controller
Keyboard & Mouse Controller
Host Bus Interface
Configuration
VDD
234
258
236
216
218
220
Internal Clock
222
224
226
228
VBAT
VSB
238
System Wake-Up Control
Power On Timers
RTC
Clock Generator
GPIO Ports
X-Bus Extension
Controller Interface
227
Power Control
Wake-Up Events
SCI&SMI
32.768KHz
Low-F Clock
High-F Clock
I/P Ports
X-Bus Interface
XIRQ
Clock
Data
Serial
230
Embedded Controller
200

FIG. 16

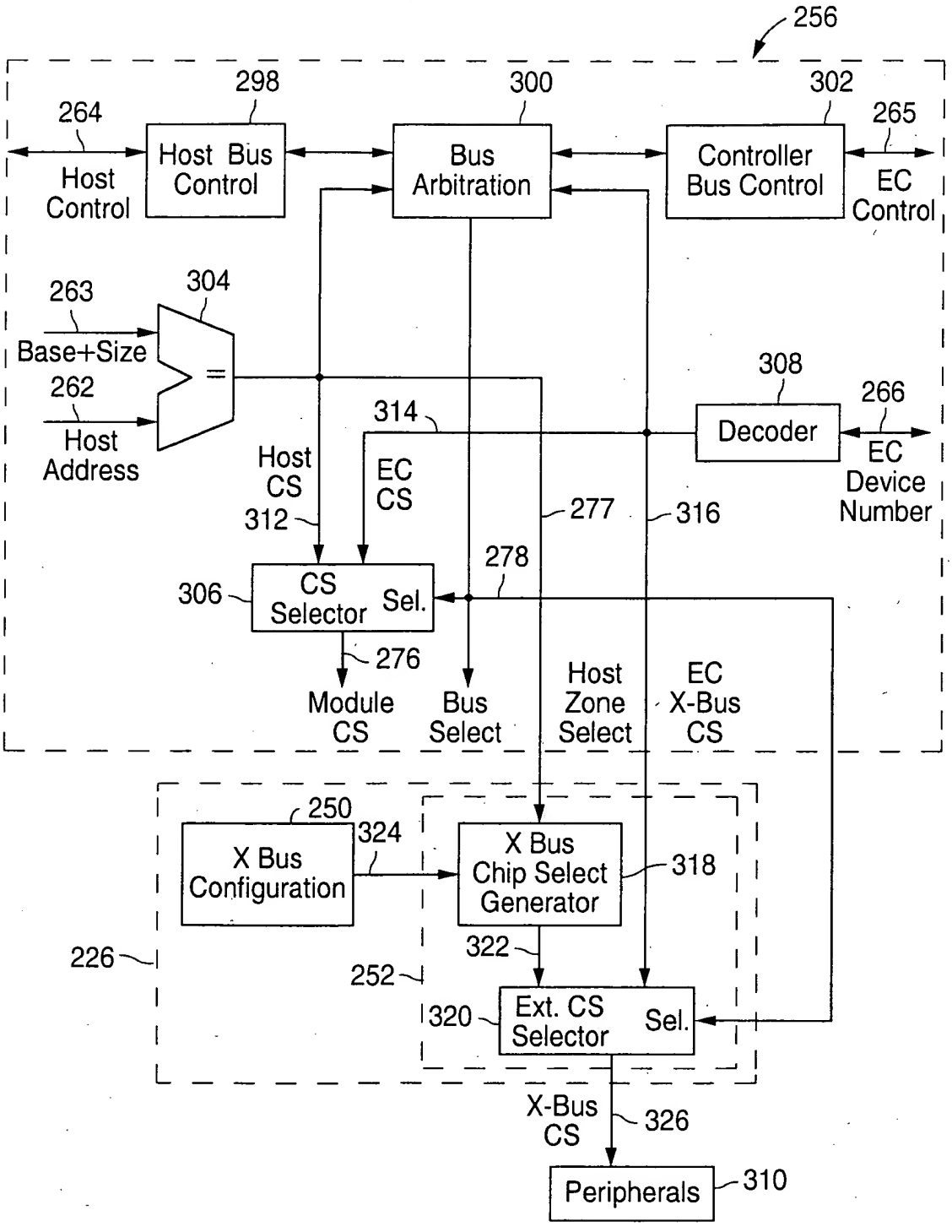
256
298
300
302
264
Host Control
Host Bus Control
Bus Arbitration
Controller Bus Control
265
EC Control
263
Base+Size
262
Host Address
304
=
308
Decoder
266
EC Device Number
314
Host CS
312
EC CS
277
316
278
306
CS Selector
Sel.
276
Module CS
Bus Select
Host Zone Select
EC X-Bus CS
250
X Bus Configuration
324
X Bus Chip Select Generator
318
226
322
252
320
Ext. CS Selector
Sel.
X-Bus CS
326
Peripherals
310

FIG. 17

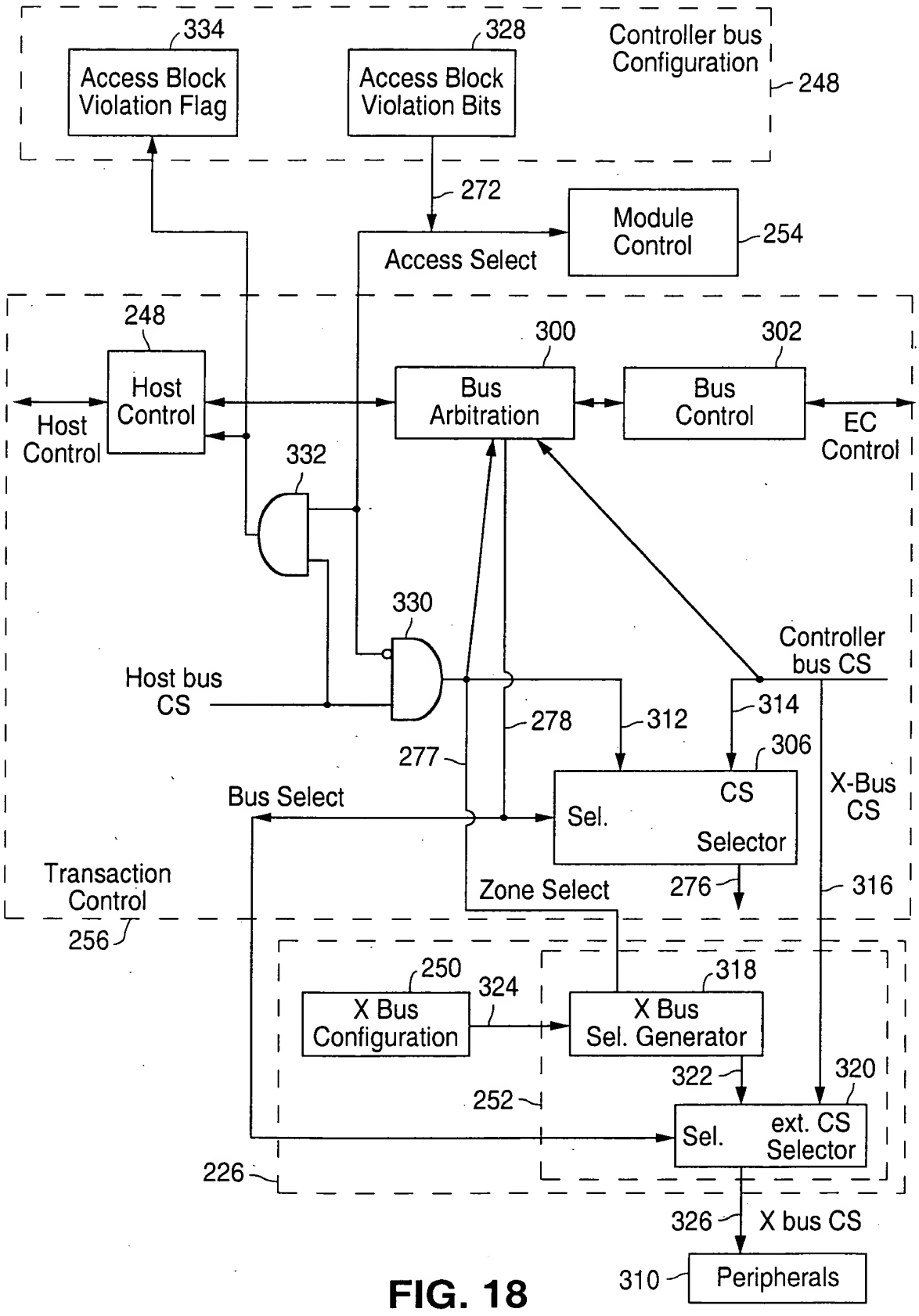
334
Access Block Violation Flag
328
Access Block Violation Bits
Controller bus Configuration
248
272
Access Select
Module Control
254
248
Host Control
Host Control
300
Bus Arbitration
302
Bus Control
EC Control
332
330
Host bus CS
Controller bus CS
314
278
312
277
306
Bus Select
CS Sel. Selector
X-Bus CS
Transaction Control
256
Zone Select
276
316
250
X Bus Configuration
324
318
X Bus Sel. Generator
322
320
252
Sel. ext. CS Selector
226
326
X bus CS
310
Peripherals

FIG. 18

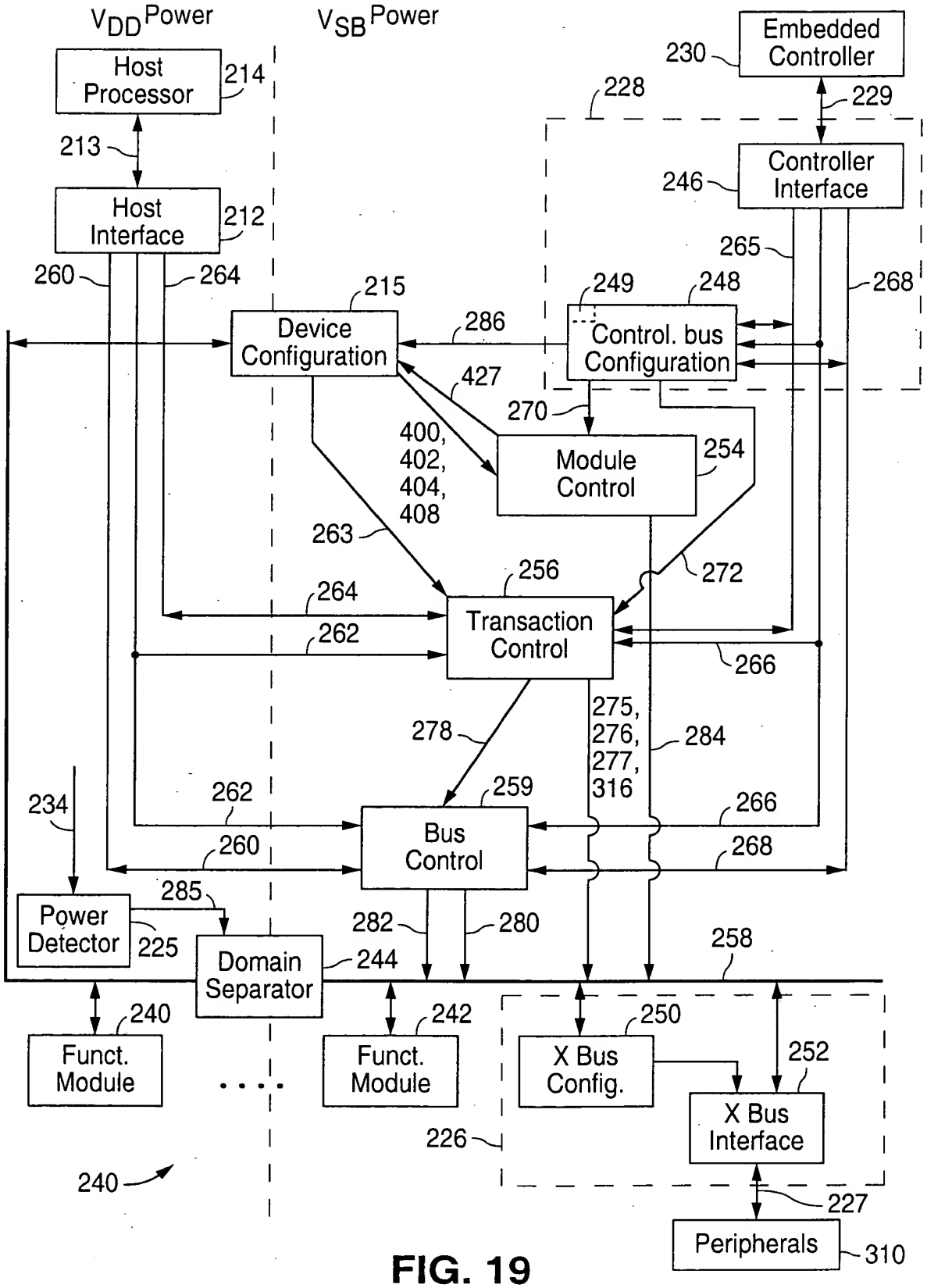
V_{DD} Power
V_{SB} Power
Host Processor
214
213
Host Interface
212
260
264
Embedded Controller
230
228
229
Controller Interface
246
265
268
249
248
215
Device Configuration
286
Control. bus Configuration
427
270
400, 402, 404, 408
Module Control
254
263
272
256
264
Transaction Control
262
266
275, 276, 277, 316
278
284
234
262
259
266
Bus Control
260
268
285
Power Detector
225
282
280
258
Domain Separator
244
240
242
250
252
Funct. Module
Funct. Module
X Bus Config.
X Bus Interface
226
240
227
Peripherals
310

FIG. 19

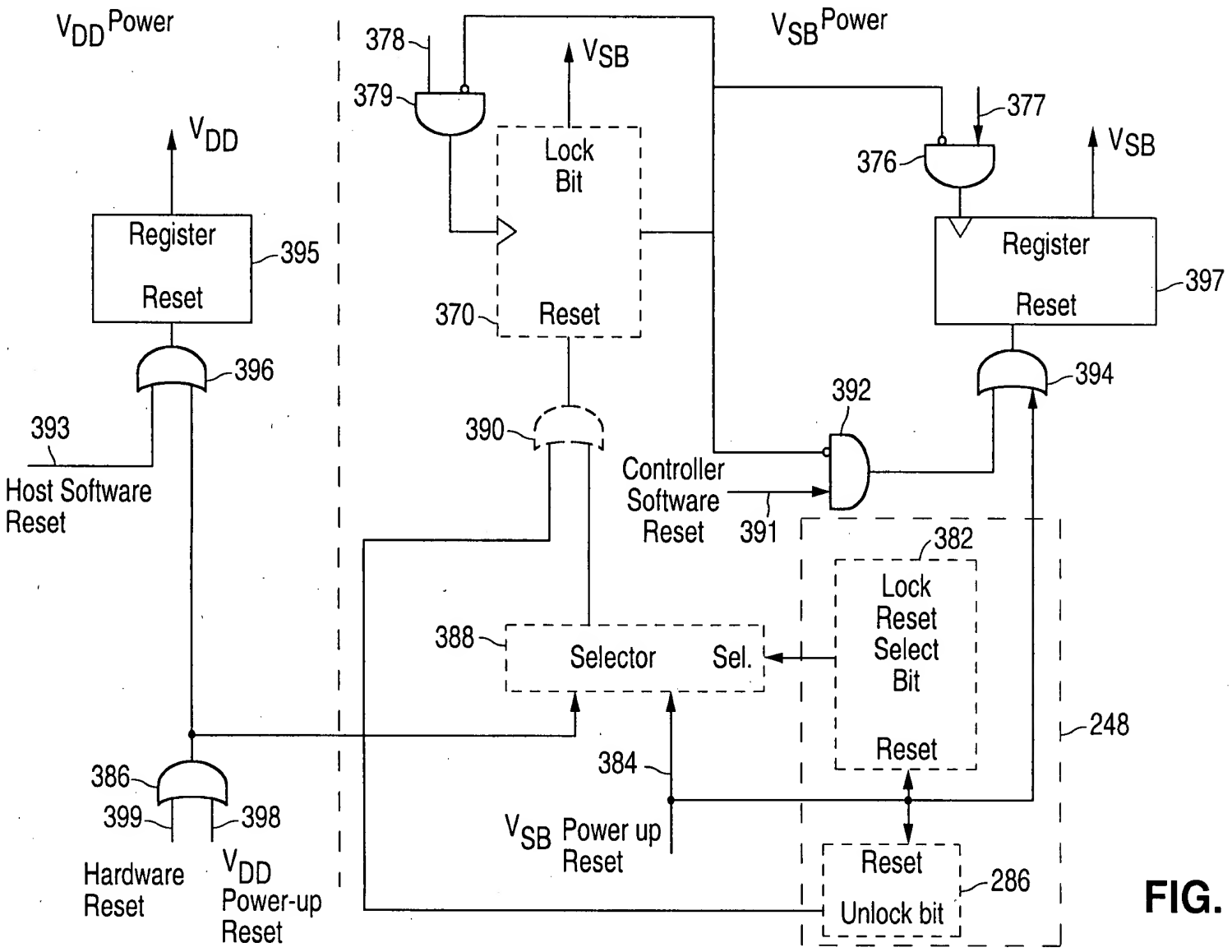
V_{DD} Power
V_{SB} Power
378
379
V_{SB}
377
376
V_{DD}
V_{SB}
Lock Bit
Register
Reset
395
370
Reset
Register
Reset
397
396
394
392
390
393
Host Software Reset
Controller Software Reset
391
382
Lock Reset Select Bit
388
Selector
Sel.
248
Reset
386
384
399
398
V_{SB} Power up Reset
Reset
Unlock bit
286
Hardware Reset
V_{DD} Power-up Reset

FIG. 20

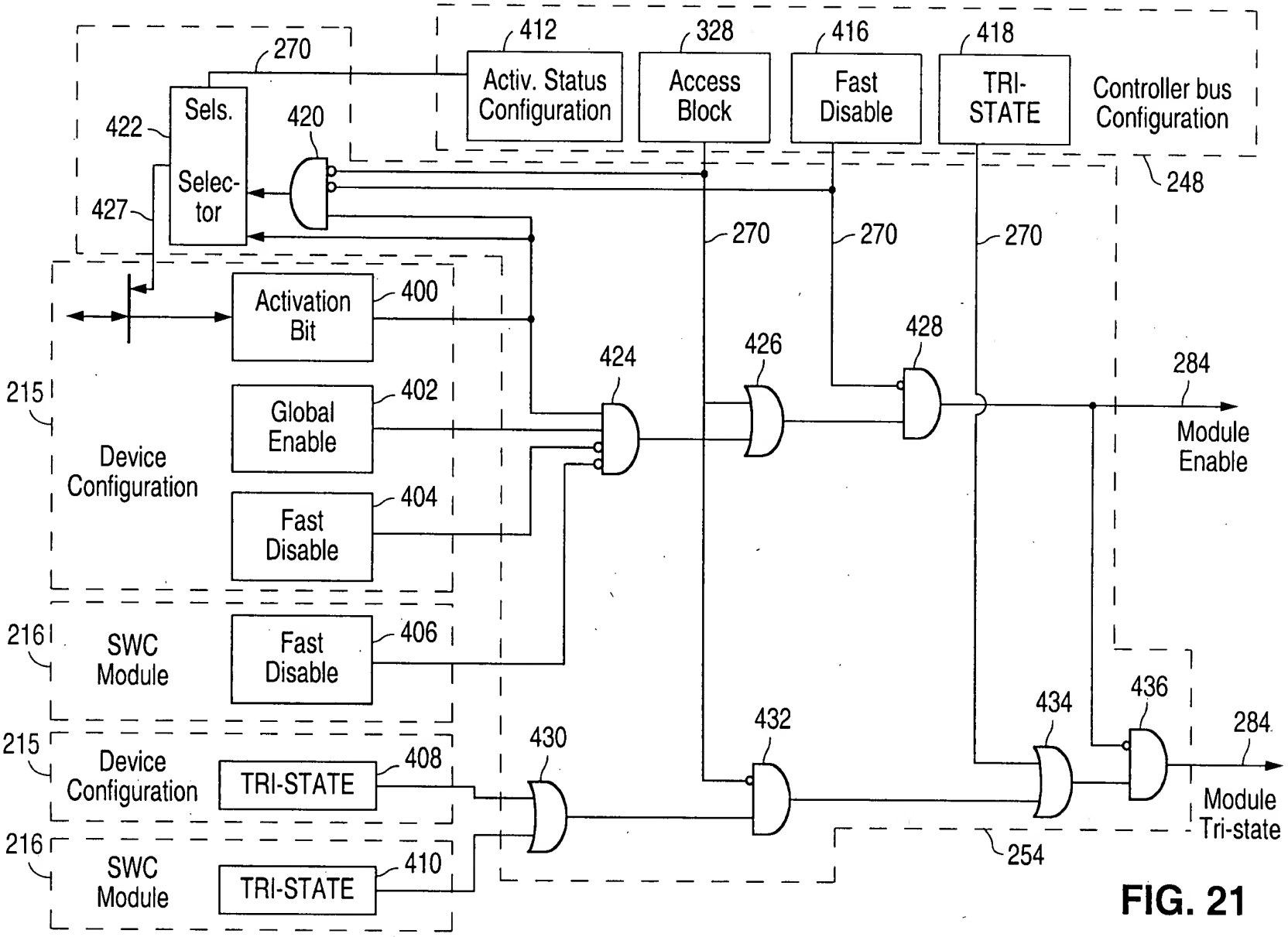
270
412
328
416
418
Activ. Status Configuration
Access Block
Fast Disable
TRI-STATE
Controller bus Configuration
248
422
Sels.
Selec-tor
420
427
270
270
270
Activation Bit
400
424
426
428
284
215
Global Enable
402
Module Enable
Device Configuration
Fast Disable
404
216
SWC Module
Fast Disable
406
215
Device Configuration
TRI-STATE
408
430
432
434
436
284
216
SWC Module
TRI-STATE
410
Module Tri-state
254

FIG. 21

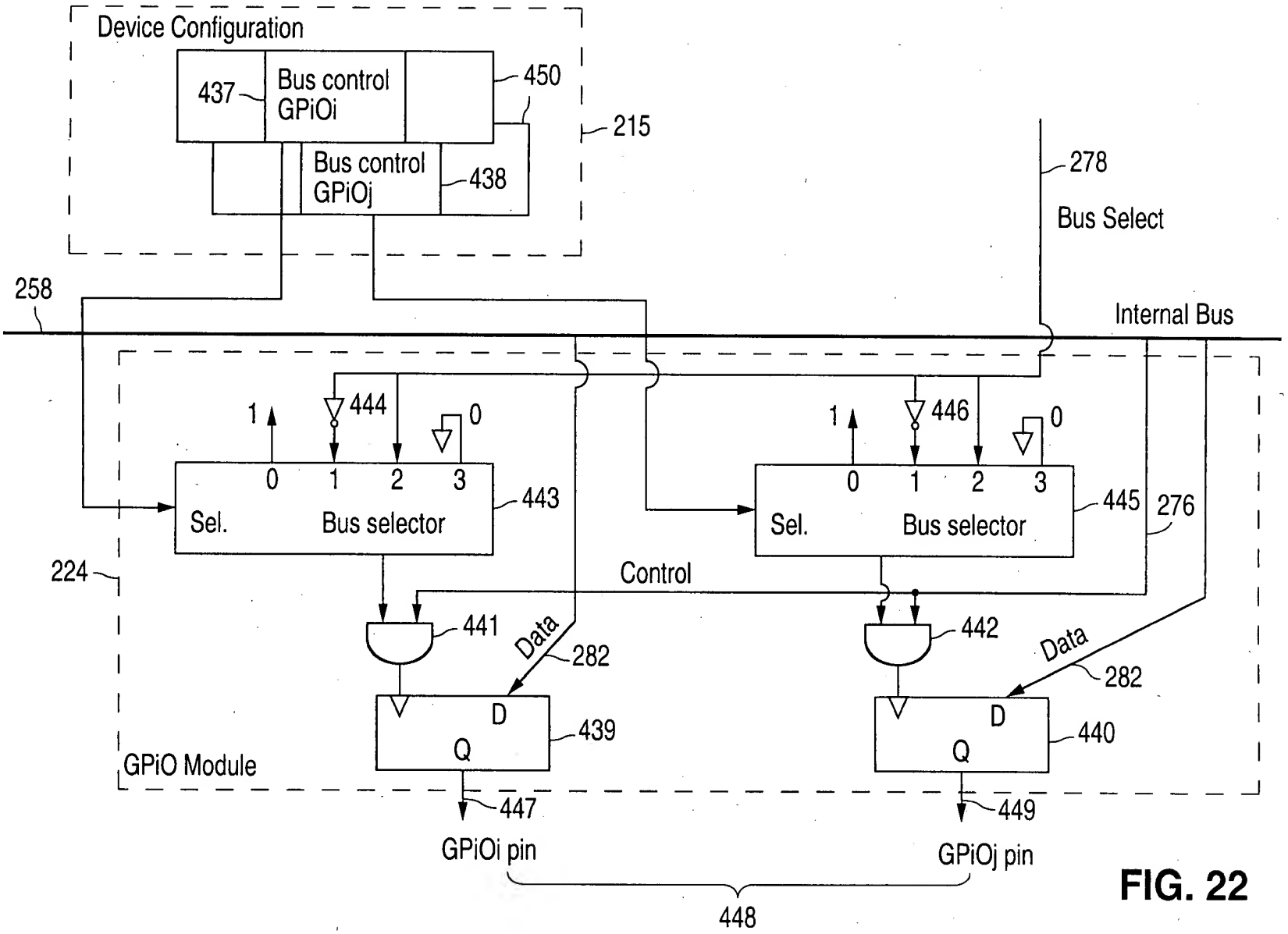
Device Configuration
437
Bus control GPiOi
450
215
Bus control GPiOj
438
278
Bus Select
258
Internal Bus
1
444
0
0 1 2 3
Sel.
Bus selector
443
1
446
0
0 1 2 3
Sel.
Bus selector
445
276
224
Control
441
442
Data
282
Data
282
D
Q
439
D
Q
440
GPiO Module
447
449
GPiOi pin
GPiOj pin
448

FIG. 22

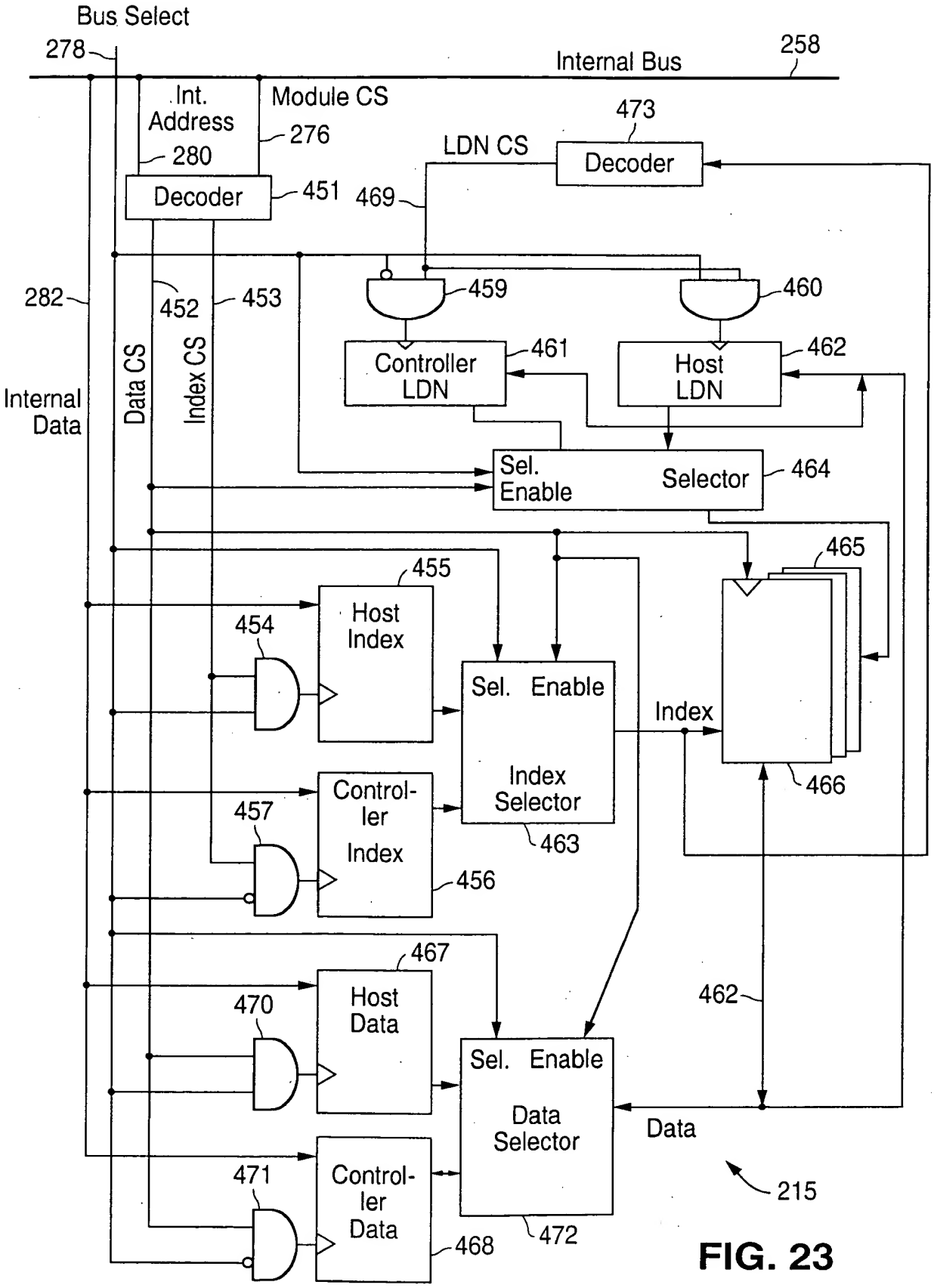
Bus Select
278
Internal Bus
258
Int. Address
280
Module CS
276
Decoder
451
469
LDN CS
473
Decoder
282
452
453
459
460
Data CS
Index CS
Internal Data
Controller LDN
461
Host LDN
462
Sel. Enable
Selector
464
465
455
Host Index
454
Sel. Enable
Index Selector
463
Index
466
Control-ler Index
457
456
467
Host Data
470
462
Sel. Enable
Data Selector
Data
471
Control-ler Data
468
472
215

FIG. 23

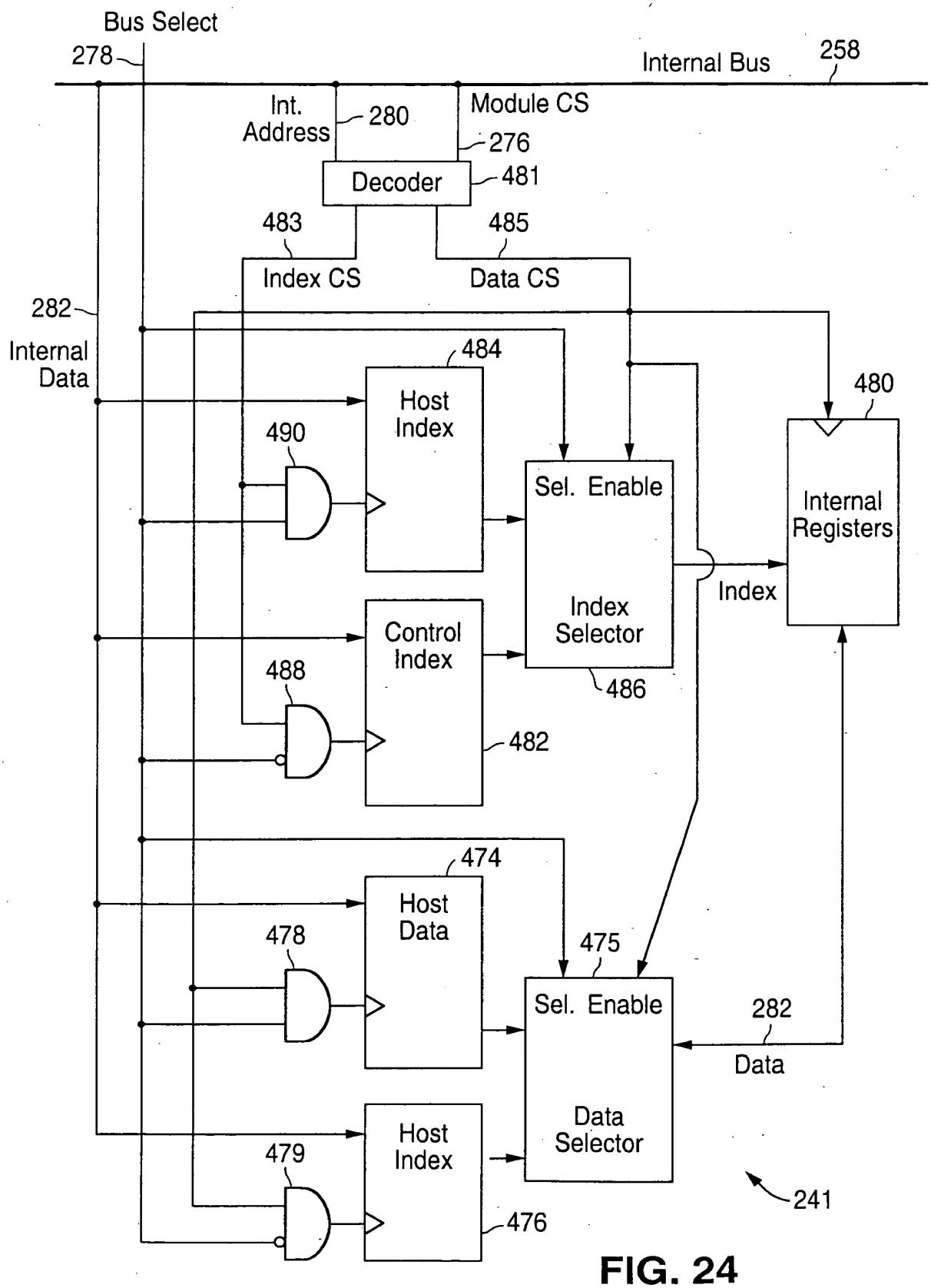
Bus Select
278
Internal Bus
258
Int. Address
280
Module CS
276
Decoder
481
483
Index CS
485
Data CS
282
Internal Data
484
Host Index
490
480
Sel. Enable
Internal Registers
Index
Index Selector
486
Control Index
488
482
474
Host Data
478
475
Sel. Enable
282
Data
Data Selector
Host Index
479
476
241

FIG. 24

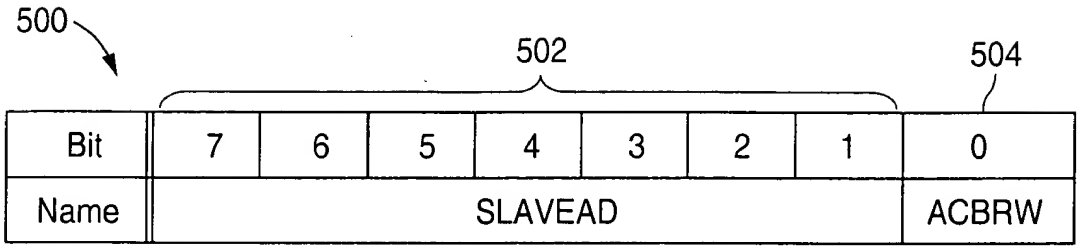

FIG. 25A

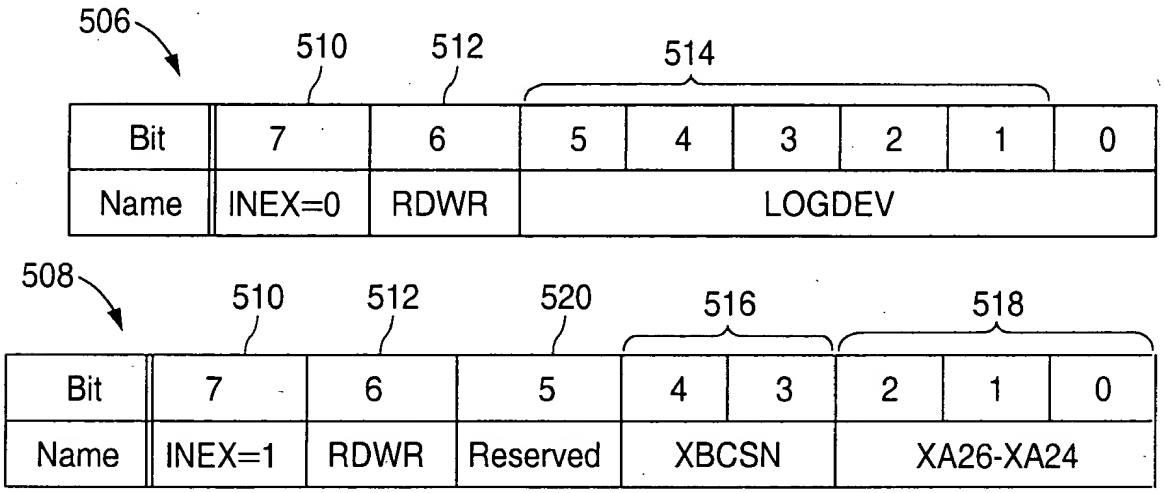

FIG. 25B

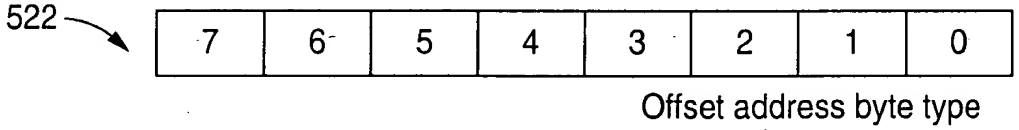

FIG. 25C

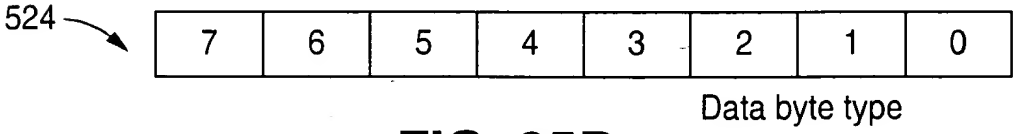

FIG. 25D

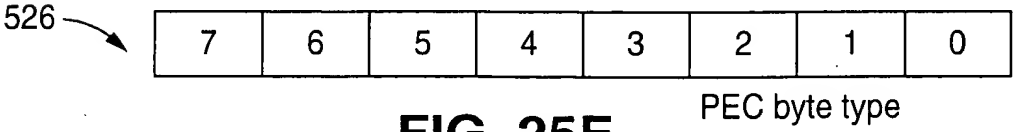

FIG. 25E

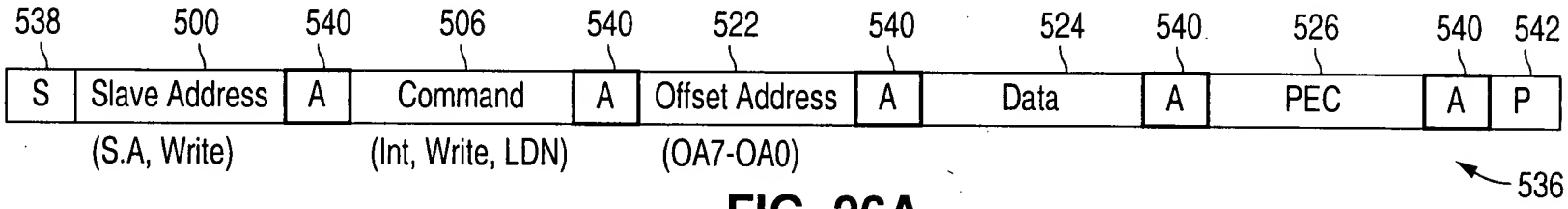

FIG. 26A

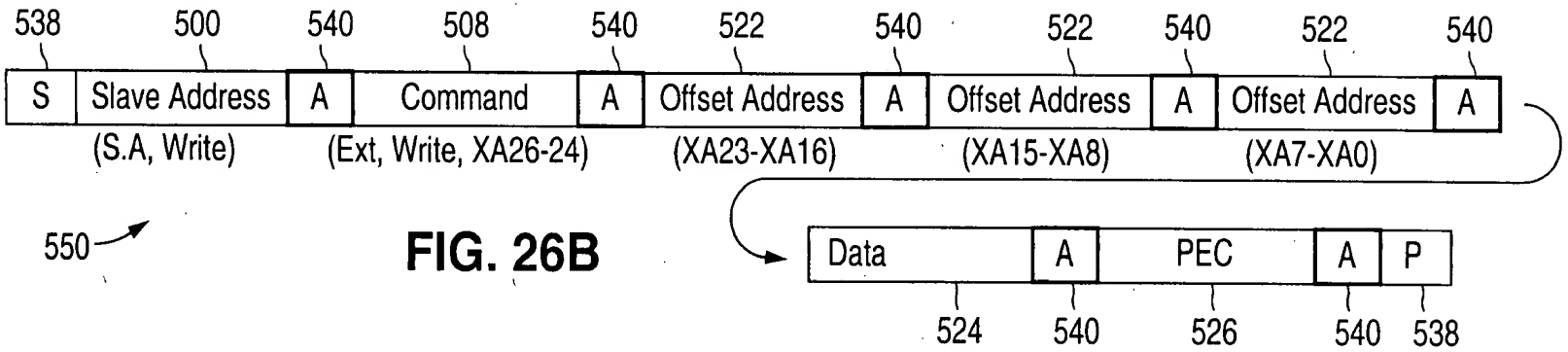

FIG. 26B

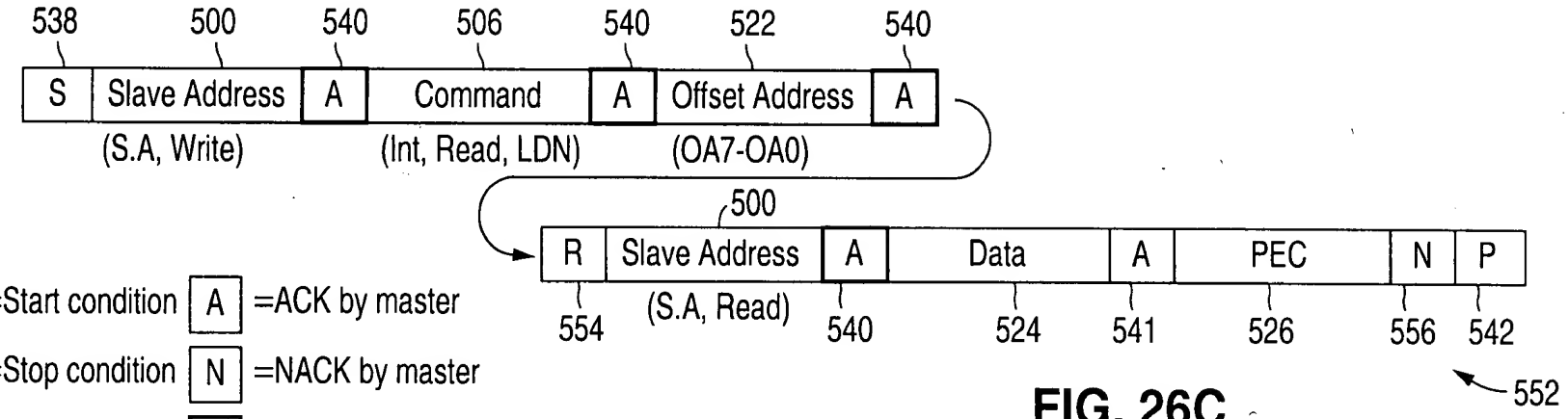

FIG. 26C

S =Start condition A =ACK by master

P =Stop condition N =NACK by master

R =Restart cond. A =ACK by slave

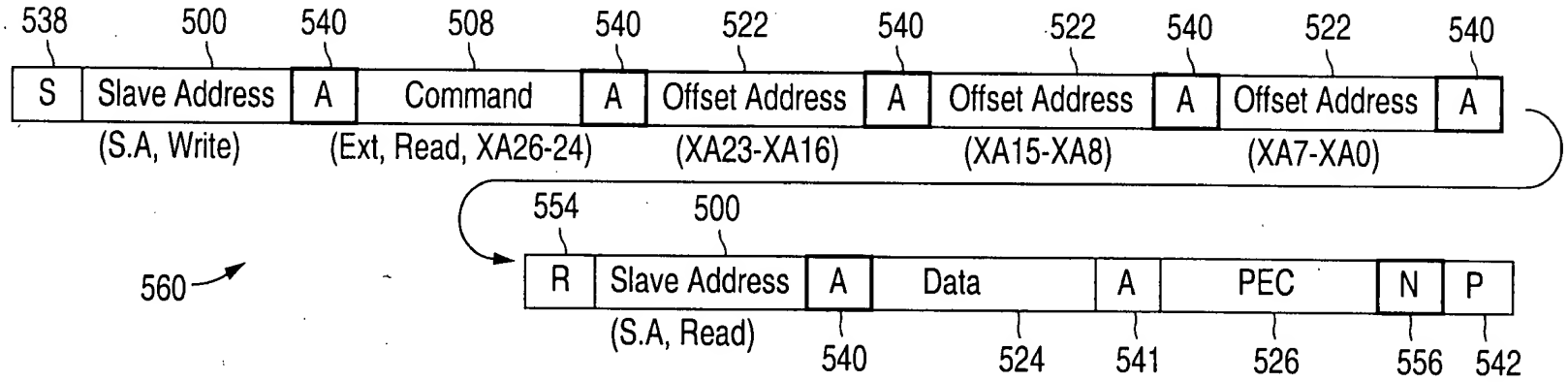

FIG. 26D

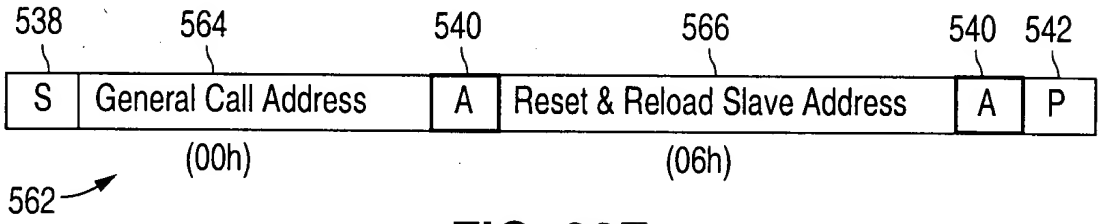

FIG. 26E

S =Start condition

P =Stop condition

R =Restart condition

A =ACK by master

N =NACK by master

A =ACK by slave

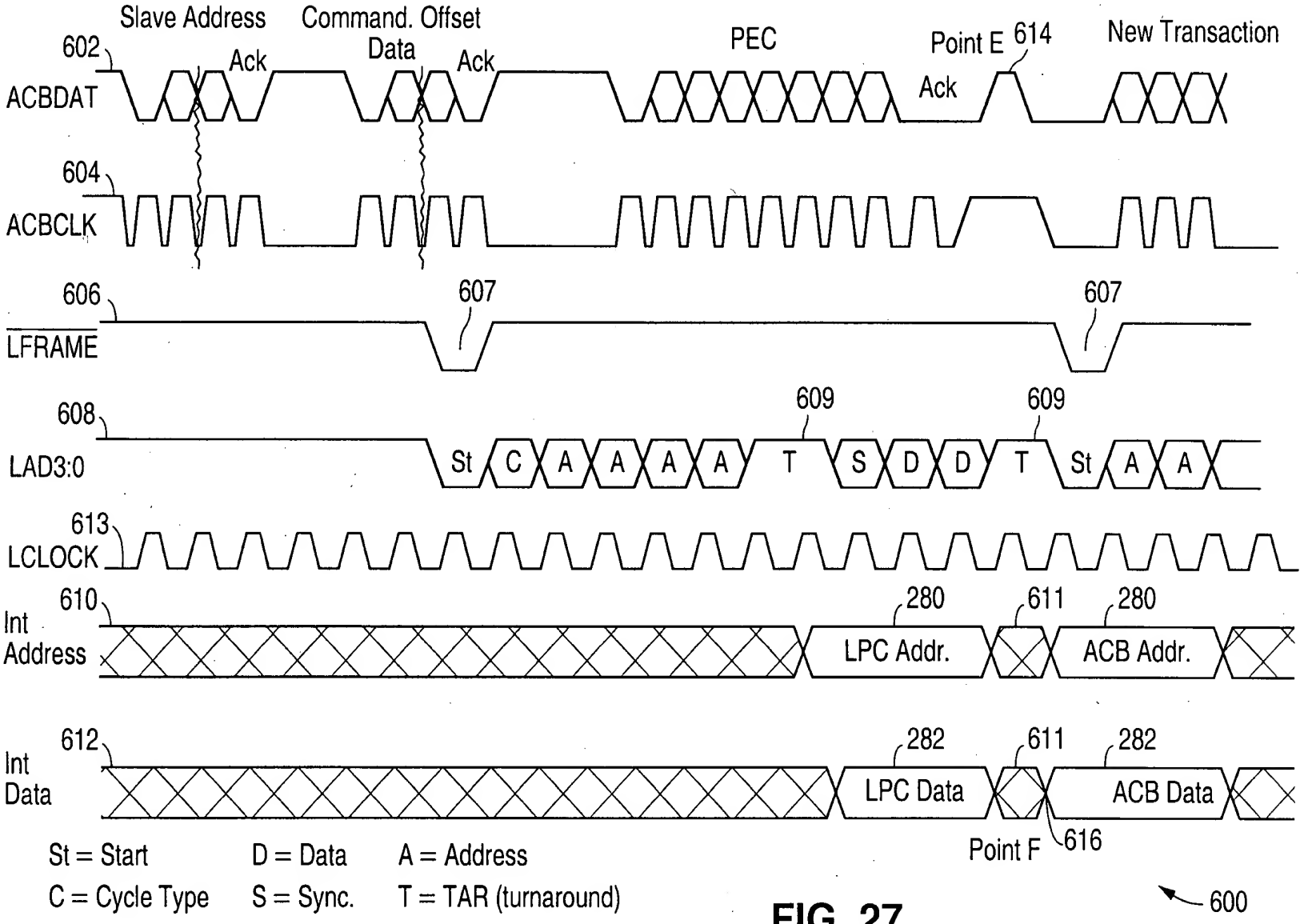
Slave Address
Command. Offset
Data
Ack
Ack
PEC
Point E
614
Ack
New Transaction
602
ACBDAT
604
ACBCLK
606
LFRAME
607
607
608
LAD3:0
609
609
St
C
A
A
A
A
T
S
D
D
T
St
A
A
613
LCLOCK
610
Int
Address
280
611
280
LPC Addr.
ACB Addr.
612
Int
Data
282
611
282
LPC Data
ACB Data
Point F
616
St = Start
D = Data
A = Address
C = Cycle Type
S = Sync.
T = TAR (turnaround)
600

FIG. 27

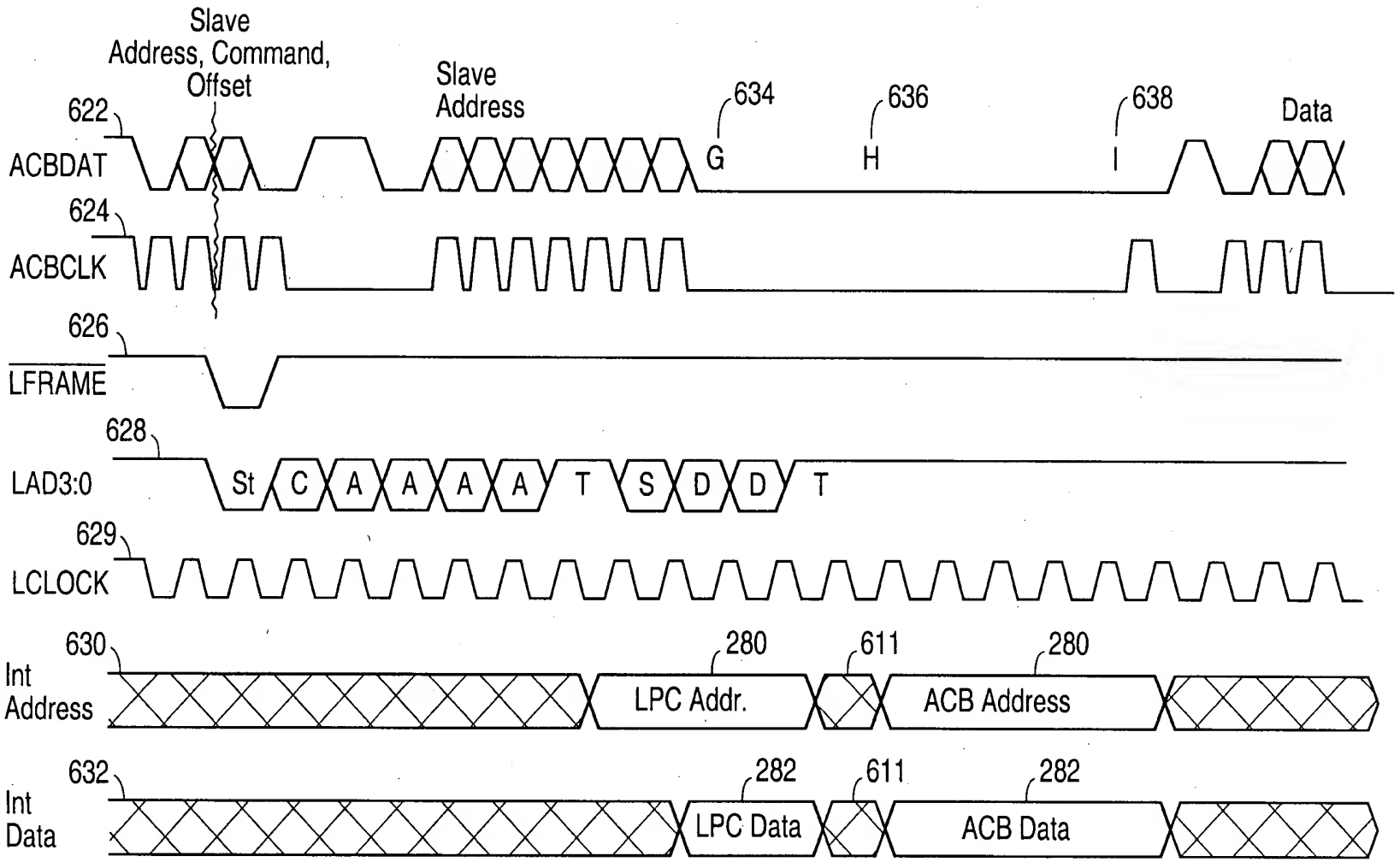
Slave
Address, Command,
Offset
Slave
Address
622
634
636
638
Data
ACBDAT
G
H
I
624
ACBCLK
626
LFRAME
628
LAD3:0
St
C
A
A
A
A
T
S
D
D
T
629
LCLOCK
630
280
611
280
Int
Address
LPC Addr.
ACB Address
632
282
611
282
Int
Data
LPC Data
ACB Data
St = Start
T = TAR (turnaround)
D = Data
C = Cycle Type
A = Address
S = Sync.
620

FIG. 28

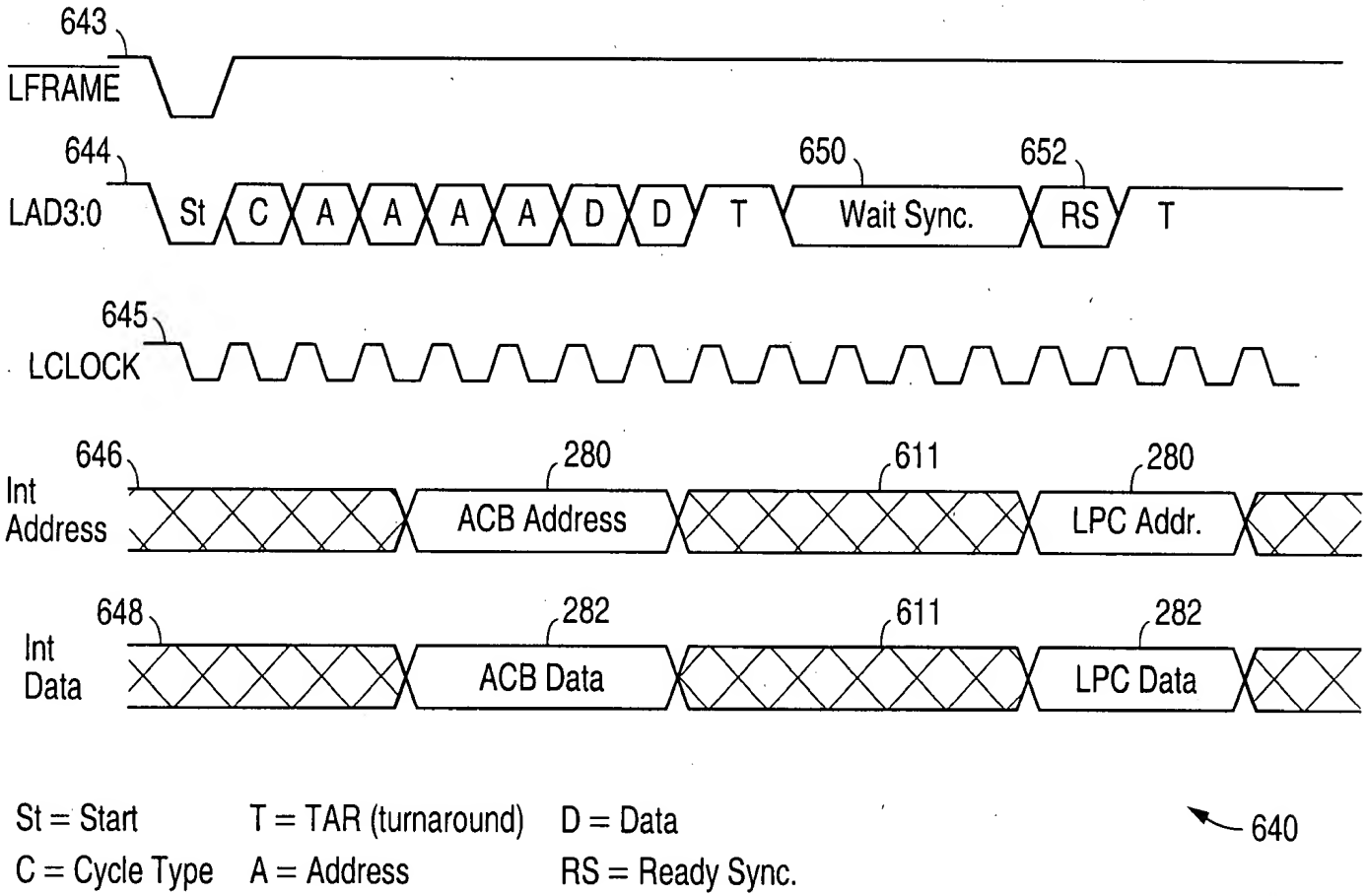
643
LFRAME
644
650
652
LAD3:0
St
C
A
A
A
A
D
D
T
Wait Sync.
RS
T
645
LCLOCK
646
280
611
280
Int
Address
ACB Address
LPC Addr.
648
282
611
282
Int
Data
ACB Data
LPC Data
St = Start
T = TAR (turnaround)
D = Data
C = Cycle Type
A = Address
RS = Ready Sync.
640

FIG. 29

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ohad Falik, et al.
Serial No.:	09/810,746
Filed:	March 16, 2001
For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

APPENDIX C -

Copy of U.S. Patent Publication 2002/0133655

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.:	09/810,746
Filed:	March 16, 2001
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Examiner:	Donna K. Mason

APPENDIX D -
Evidence Appendix

Sun Microsystems Press Release, February 19, 1998.

SUN MICROSYSTEMS UNVEILS NEW SPARCENGINE COMPACTPCI FAMILY OF EMBEDDED-BOARD COMPUTERS

New Boards Provide Telecom and Embedded Customers Most Comprehensive Solution

STUTTGART, Germany. - February 18, 1998 - Sun Microsystems, Inc. today announced the SPARCengine™ CP 1200 and CP 1500, two embedded-board computers for mission critical telecom and industrial computing applications. These new boards are an extension of Sun's offerings in the telecom and industrial computing markets and represent Sun's first CompactPCI (cPCI) based offering.

"As a leading, world-wide supplier of telecommunications equipment, we welcome Sun's entry into the CompactPCI market," said Jorma Mobrin, vice president, Corporate Technologies, Telefonaktibolaget LM Ericsson. "The high performance provided by Sun's SPARC™ architecture, coupled with an industry standard form factor, will allow telecommunication companies to rapidly create powerful and cost effective products."

"Sun is entering the CompactPCI market from a position of strength," said Jeff Veis, Sun Microsystems' Group Marketing Manager, Platform Products. "These first two CompactPCI products address the cost-sensitive and high performance needs of the embedded marketplace. Other microprocessor platforms are not able to provide this kind of highly integrated, cPCI solution with the proven value of the SPARC processor and Solaris™ operating system (OS) combination."

SPARCengine CP Family Delivers Comprehensive Scalable Solution

The Sun™ SPARCengine CP family of cPCI board computers is designed for OEM customers with demands for High Availability embedded processing platforms that must perform under extreme conditions or meet difficult environmental specifications. Applications in this market typically require rack-mount systems with a high-speed backplane bus architecture. Sun's SPARCengine CP family provides OEM customers with real-time industrial computer applications, a complete, low-cost, highly integrated, flexible solution. In addition, the CP family delivers the advantages of an industry standard-based offering, with a high performance PCI-based solution to companies such as telecommunications and networking equipment providers, who previously depended on proprietary bus architectures.

As an executive member of the PCI Industrial Computer Manufacturers Group (PICMG), Sun fully complies with the standard for cPCI. Sun's CP family facilitates the design of mission critical applications through the sturdy packaging of the 6U Eurocard form factor, 3.3V operation, and a passive backplane architecture. Both the CP 1200 and CP 1500 feature an industry leading level of device integration including 10/100 BASE-T Ethernet, flash memory, rear panel I/O for enhanced serviceability, SCSI controllers, support for seven additional CompactPCI devices and extensive diagnostic and manufacturing test support.

Robust Software Support

The SPARCengine CP family supports Sun's Solaris 64-bit operating system and is binary-compatible with the broad array of existing SPARC applications. The binary compatibility delivered by the Solaris OS enables Sun's Dévelop and Deploy advantage, accelerating time-to-market and eliminating the need for cross compilation. OEMs can

take advantage of High Availability solutions from Sun and third parties, like the Solaris Cluster Software technology, to support mission critical applications. In addition, Real Time Operating System (RTOS) and tool chain suppliers, including VxWorks/Tornado from WindRiver, Chorus from Sun, and GNUpro from Cygnus, will be available to support embedded applications. Like all SPARC products, the SPARCengine CP family is supported by the industry's largest installed base of native RISC development environments and applications. These tools and technologies make the SPARCengine CP family ideal for embedded, telecommunications and networked computing applications.

SPARCengine CP 1500: A High-Performance, Single-slot Solution

The CP 1500 is a high-performance, single-slot cPCI board that will initially be available with Sun's 270 MHz, 64-bit UltraSPARC™-IIi microprocessor and will follow with future speed upgrades. The CP 1500 takes full advantage of the VIS™ extended instruction set, which delivers the industry's best networking and software application acceleration capabilities. The innovative board and mezzanine memory module design delivers the industry's leading single slot solution in its class. The board's low profile form factor has two significant benefits. First, it frees critical backplane expansion space in embedded system designs and second, customers can mount it as a daughter board onto existing proprietary legacy systems. The high level of integration in the microprocessor, including on-board memory controller and dual channel PCI interface, gives OEMs an immediate realization of lower total system cost while providing high performance. The CP 1500 incorporates advanced features such as dual channel 100Mbit Ethernet that is routed to both the front and back of the card and onboard Ultra-Wide SCSI controller. The CP 1500 supports up to 256MB of on board memory making it ideal for telecommunications applications like PBX, central office switches and cellular base station controllers.

SPARCengine CP 1200 Board: A Highly Integrated, Low Power Solution

The CP 1200 board takes advantage of Sun's highly integrated microSPARC-IIep microprocessor running at 100 MHz and 125 MHz. Like the CP 1500, the CP 1200 has all the components necessary to boot an operating system on board. Its 6U Eurocard form factor and integrated flash memory support make it ideal for communications applications. This board is designed to meet the cost sensitive or low power requirements in networking, telecommunications, and industrial automation and control, and is optimized for applications such as cellular base stations, storage devices, switch control processors, bridges, routers, and transmission systems.

Pricing and Availability

The SPARCengine CP 1200 board is now sampling with volume production within the second calendar quarter of 1998. Individual boards sell for less than $1,500 in quantities of 500. The CP 1500 CPCI board, with a 64MB memory module, is scheduled to sample in April, with volume availability mid-year, and sells for less than $7000 in quantities of 500. For further information about Sun's CPCI products contact Sun Microelectronics Sales at US (800) 681-8845 or international +1 (512) 434-1503. For more information visit our Web site at http://www.sun.com/microelectronics.

About Sun

Since its inception in 1982, a singular vision, "The Network Is The Computer™," has propelled Sun Microsystems, Inc. (NASDAQ:SUNW) to its position as a leading provider of hardware, software and services for establishing enterprise-wide intranets and expanding the power of the Internet. With more than $9 billion in annual revenues, Sun can be found in more than 150 countries and on the World Wide Web at http://www.sun.com.

Press announcements and other information about Sun Microsystems are available on the Internet via the World Wide Web using a tool such as Netscape Navigator or Sun's HotJava. Type http://www.sun.com at the URL prompt.

PR Contacts for Press and Analysts:

Sun Microsystems, Inc.	Thomas Associates for Sun Microsystems, Inc.
Caroline Phillips (408) 544-0288 caroline.phillips@eng.sun.com	Roger Knott (650) 596-2700 roger@thomaspr.com

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For:	SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR
Group No.:	2111
Examiner:	Donna K. Mason

APPENDIX E -

Related Proceedings Appendix

Not Applicable – To the best knowledge and belief of the undersigned attorney, there are none.